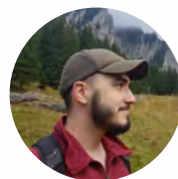
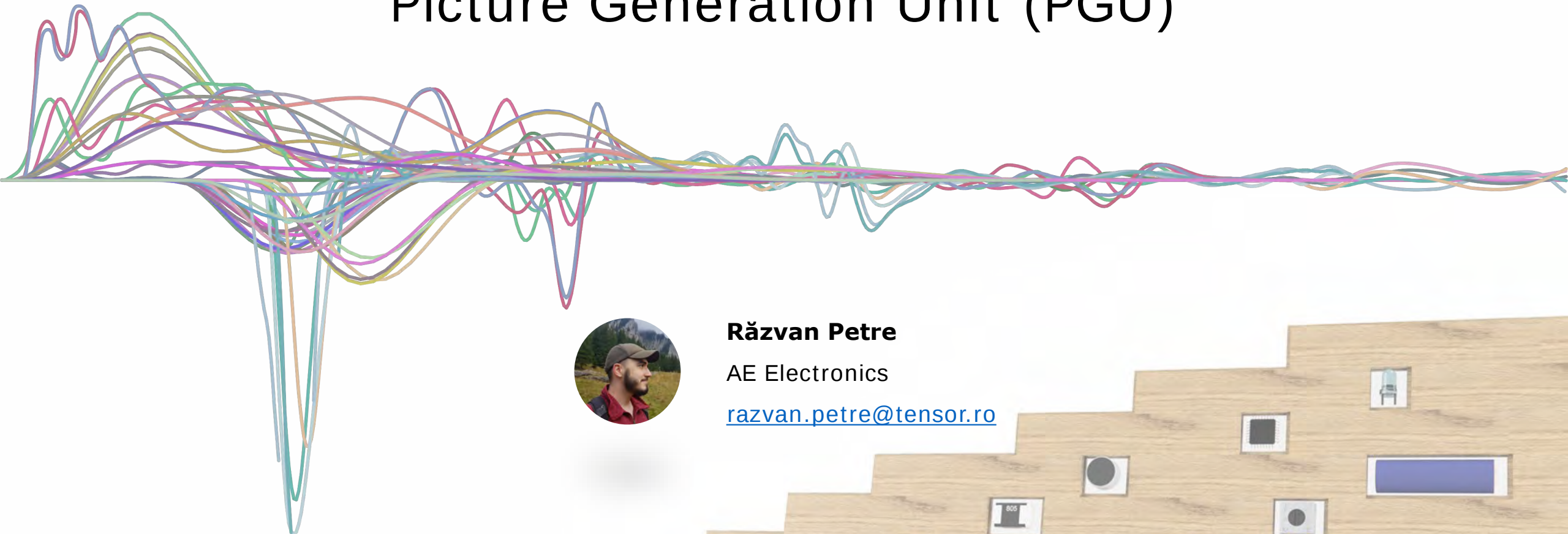


TIEplus 2020 challenge

Picture Generation Unit (PGU)



Răzvan Petre

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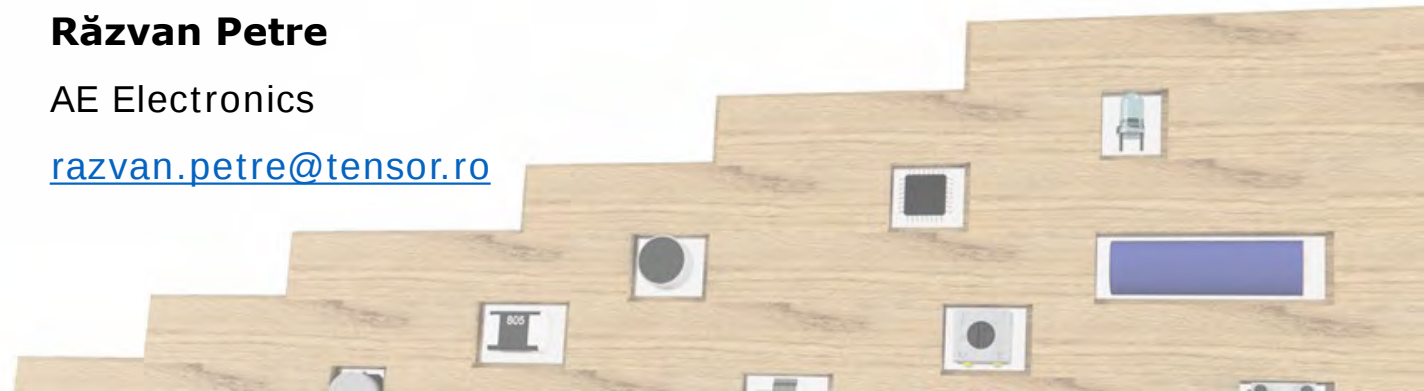


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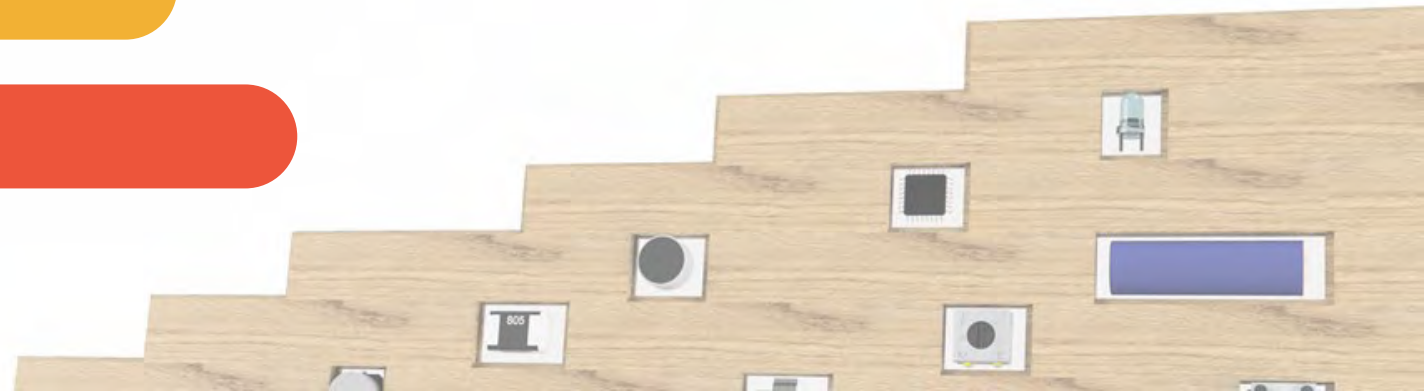
Power Integrity – pre-layout

6

Power Integrity – post-layout

7

Conclusions



Picture Generation Unit (PGU)

- IC1000: Power Supply
- IC2000: Display Controller
- IC3000: Digital Mirror Device

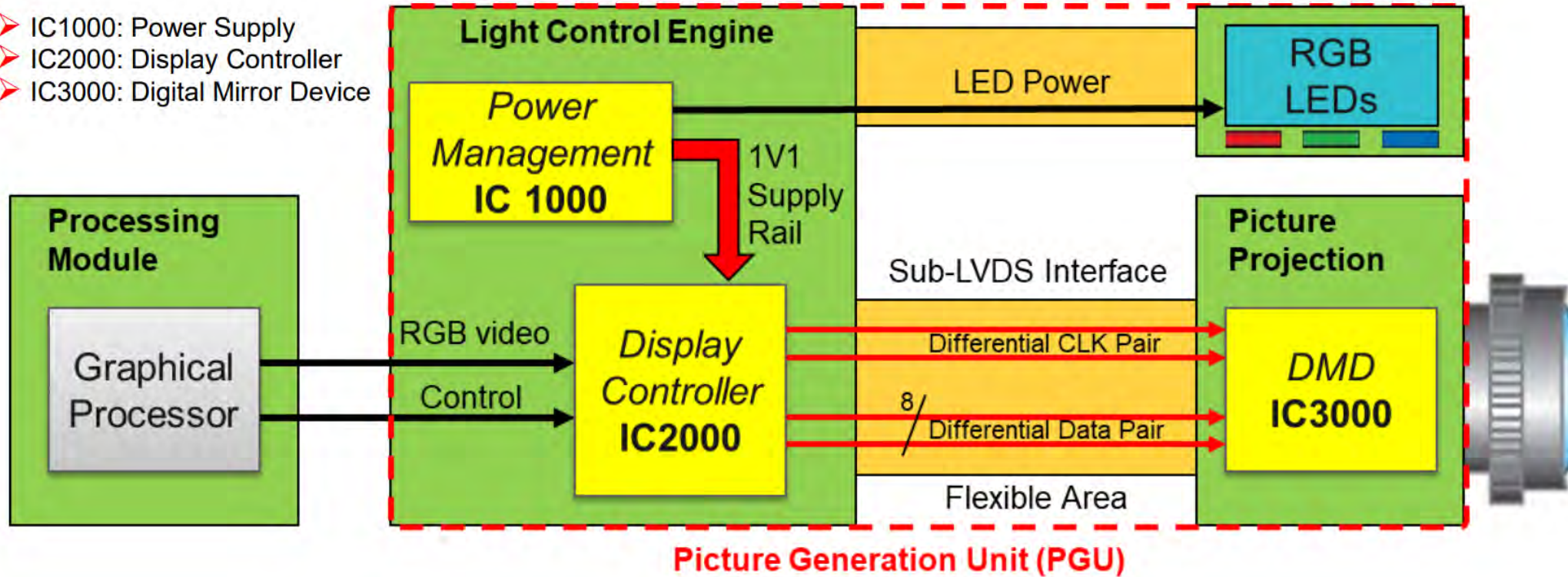
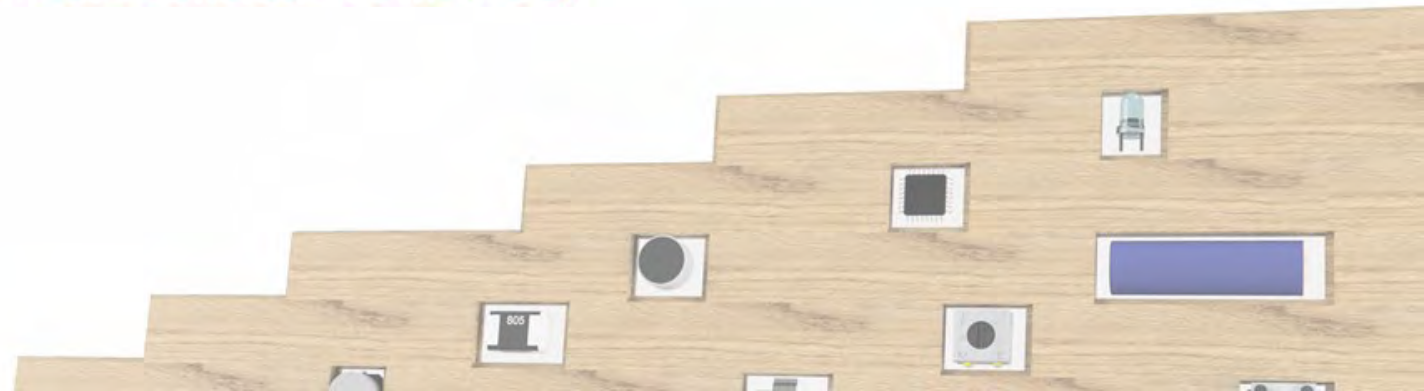
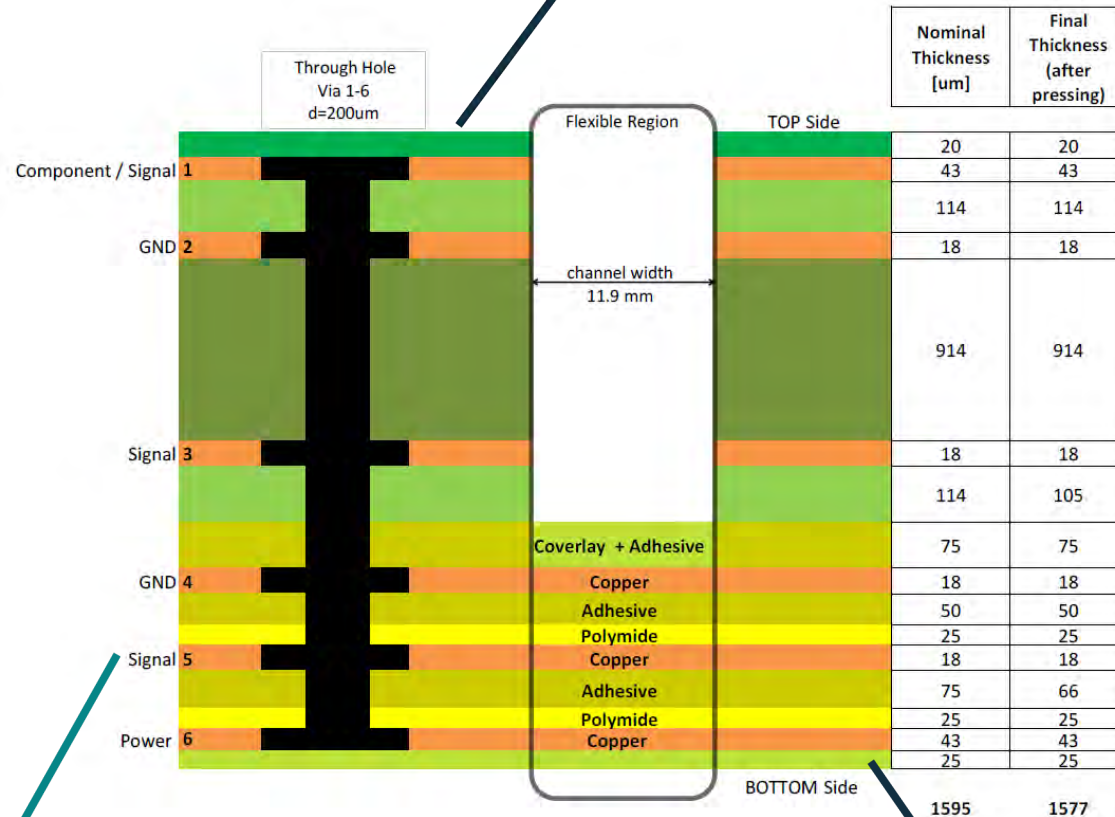


Figure 1 – Block Schematic



1 General aspects

Picture Generation Unit (PGU)



IC1000
IC2000

GND
plane

Power
plane(s)

IC3000

Sub-LVDS

Figure 2 – PCB Stack-up



Equivalent Thermal Network

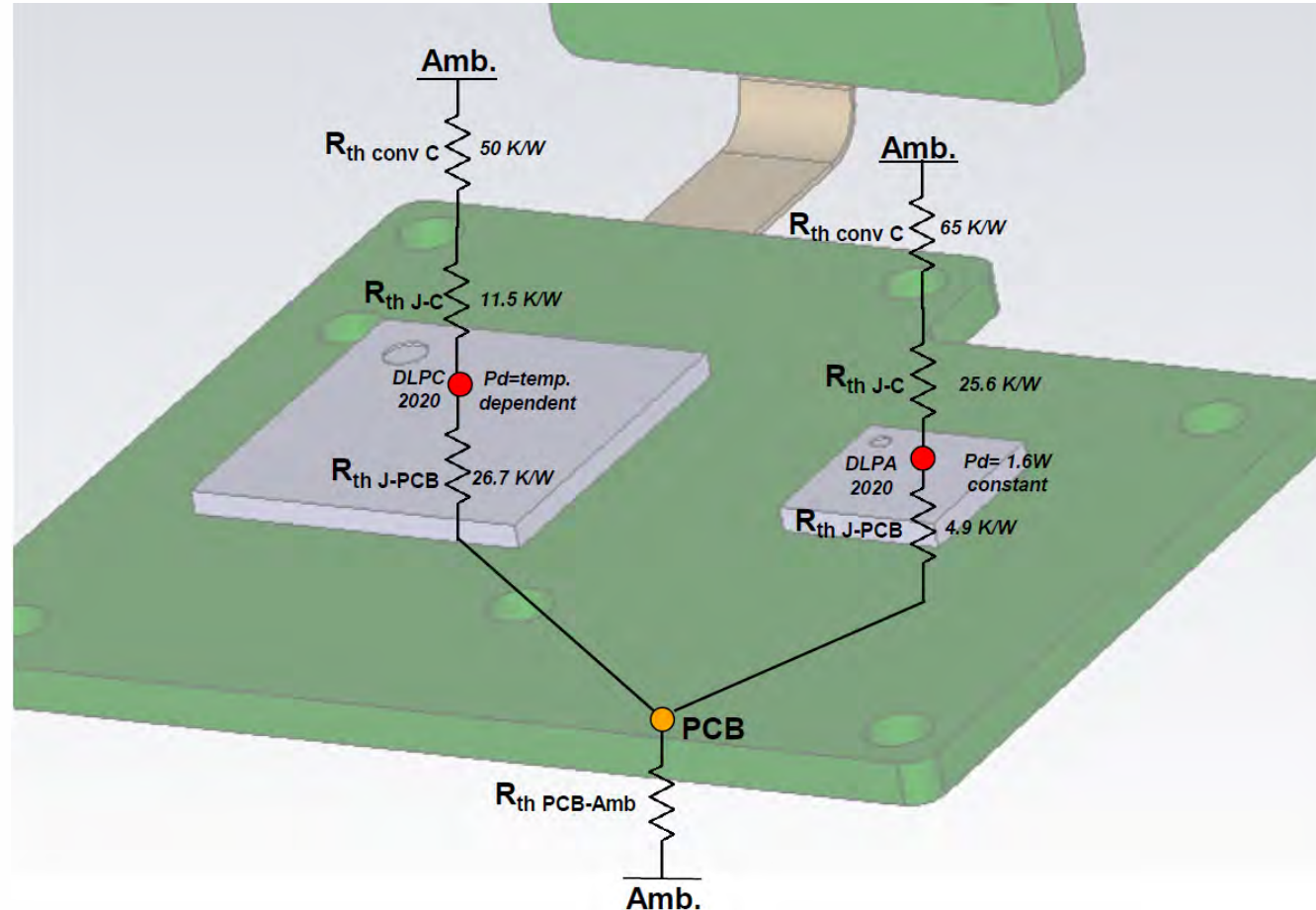


Figure 3 – Equivalent Thermal Network



Equivalent Thermal Network - preliminary

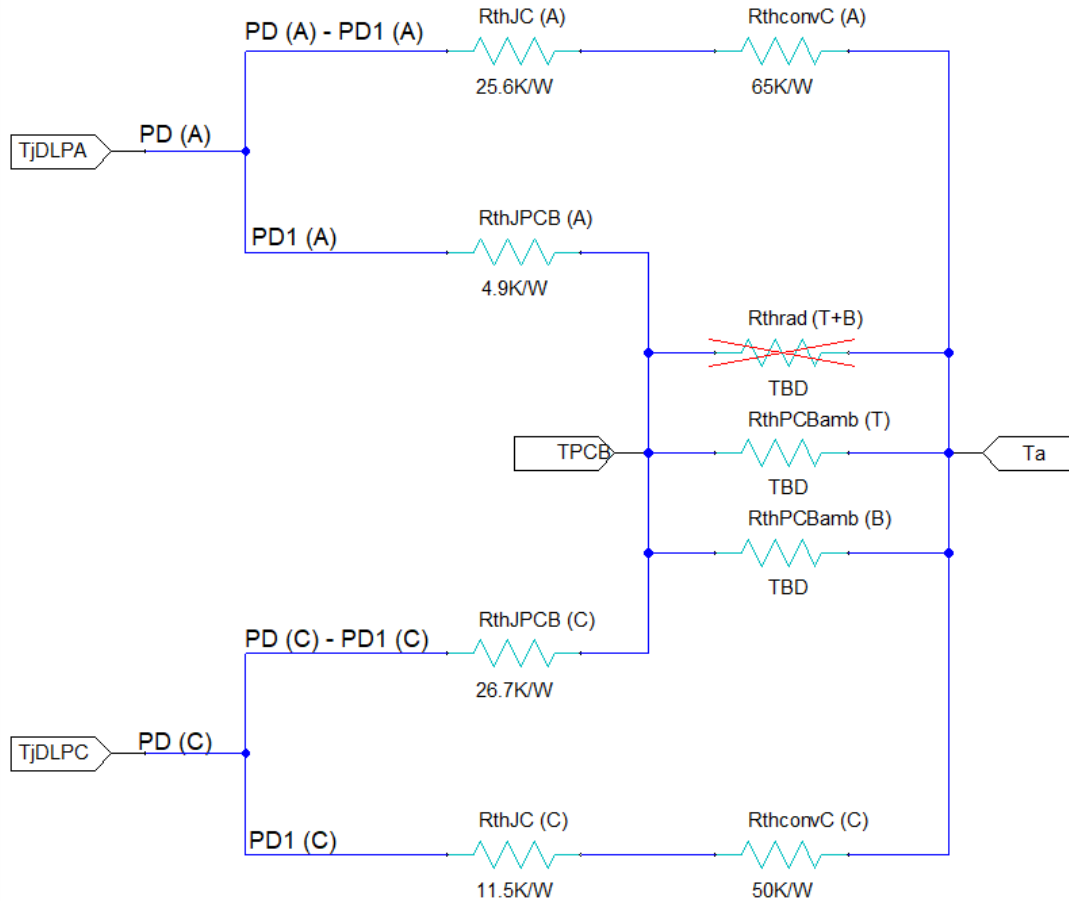


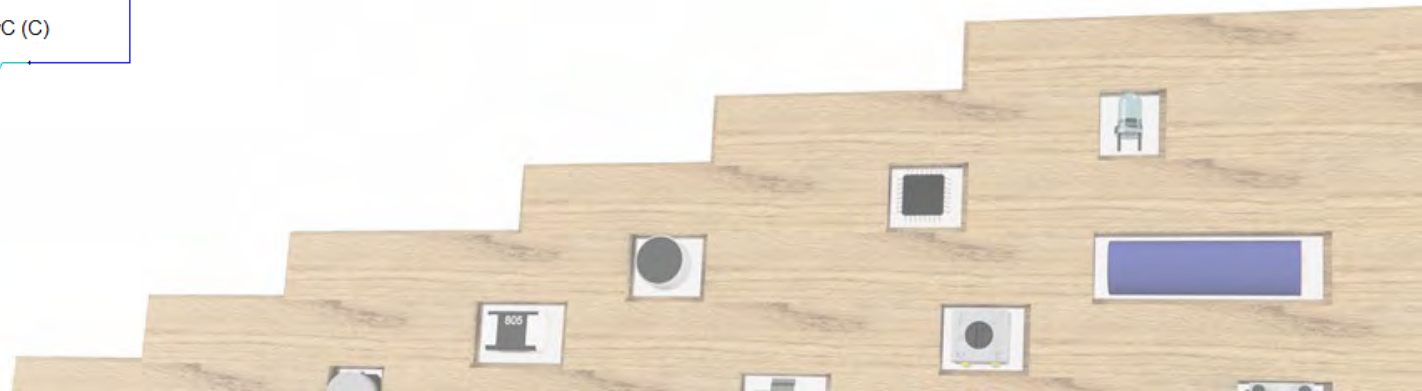
Figure 4 – Equivalent Thermal Network – preliminary

$$\begin{cases} R_{thPCBamb}(T) = \frac{1}{h_{TOP} \cdot A_{TOP}} \\ R_{thPCBamb}(B) = \frac{1}{h_{BOTTOM} \cdot A_{BOTTOM}} \end{cases}$$

Equation 1 – Thermal resistances of convection, TOP and BOTTOM

$$\begin{cases} h_{TOP} = 1.6 \cdot (T_{PCB} - T_a)^{\frac{1}{3}} \\ h_{BOTTOM} = 0.65 \cdot \left(\frac{T_{PCB} - T_a}{A_{BOTTOM}/P} \right)^{\frac{1}{4}} \end{cases}$$

Equation 2 – Convection Coefficients, TOP and BOTTOM



Thermal Analysis results - preliminary

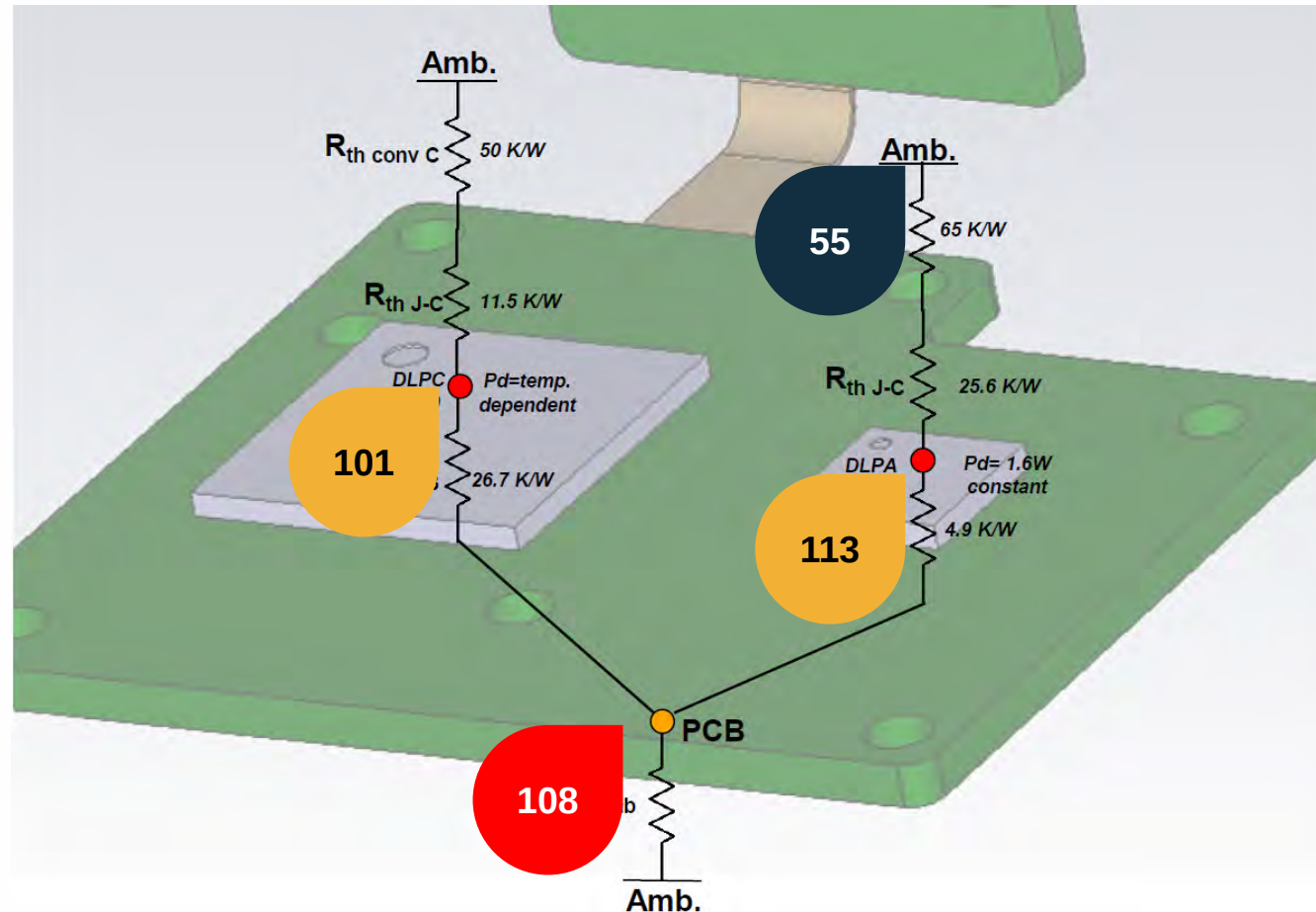


Figure 5 – Thermal Analysis results – preliminary. All temperatures in Celsius Degrees



Equivalent Thermal Network - improved

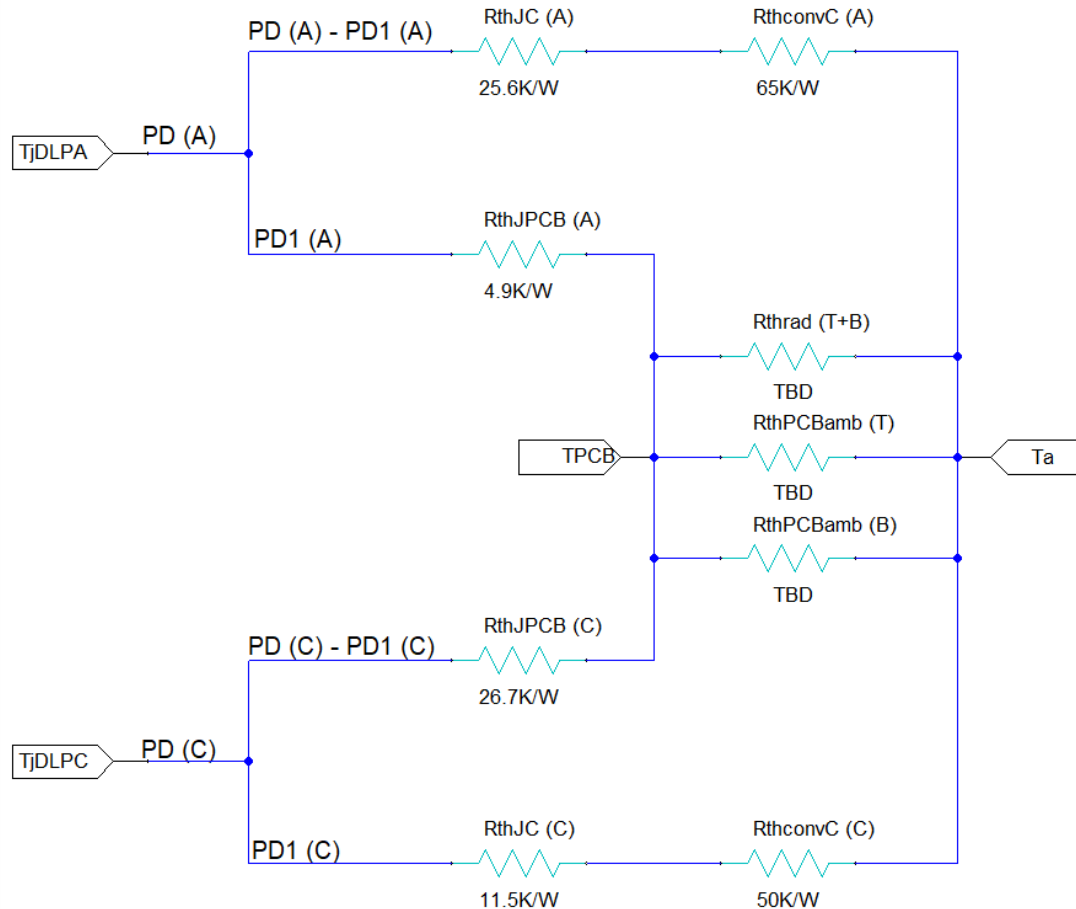


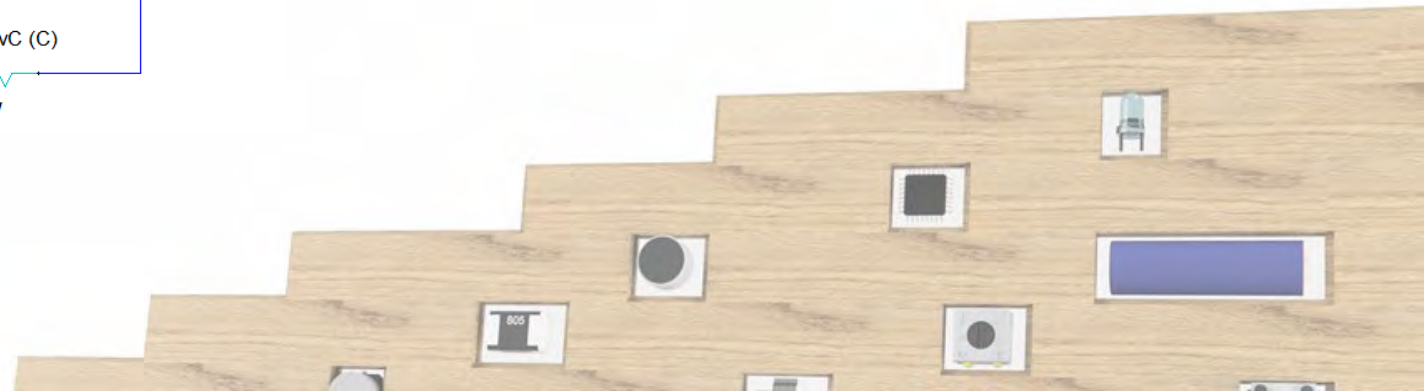
Figure 6 – Equivalent Thermal Network – improved

$$R_{thrad} = \frac{1}{\alpha_{radiation} \cdot (A_{TOP} + A_{BOTTOM})}$$

Equation 3 – Thermal resistances of radiation, TOP and BOTTOM

$$\alpha_{radiation} = \varepsilon \cdot \sigma \cdot (T_{PCB}^2 + T_a^2) \cdot (T_{PCB} + T_a)$$

Equation 4 – Coefficient of radiation, TOP and BOTTOM



Thermal Analysis results - improved

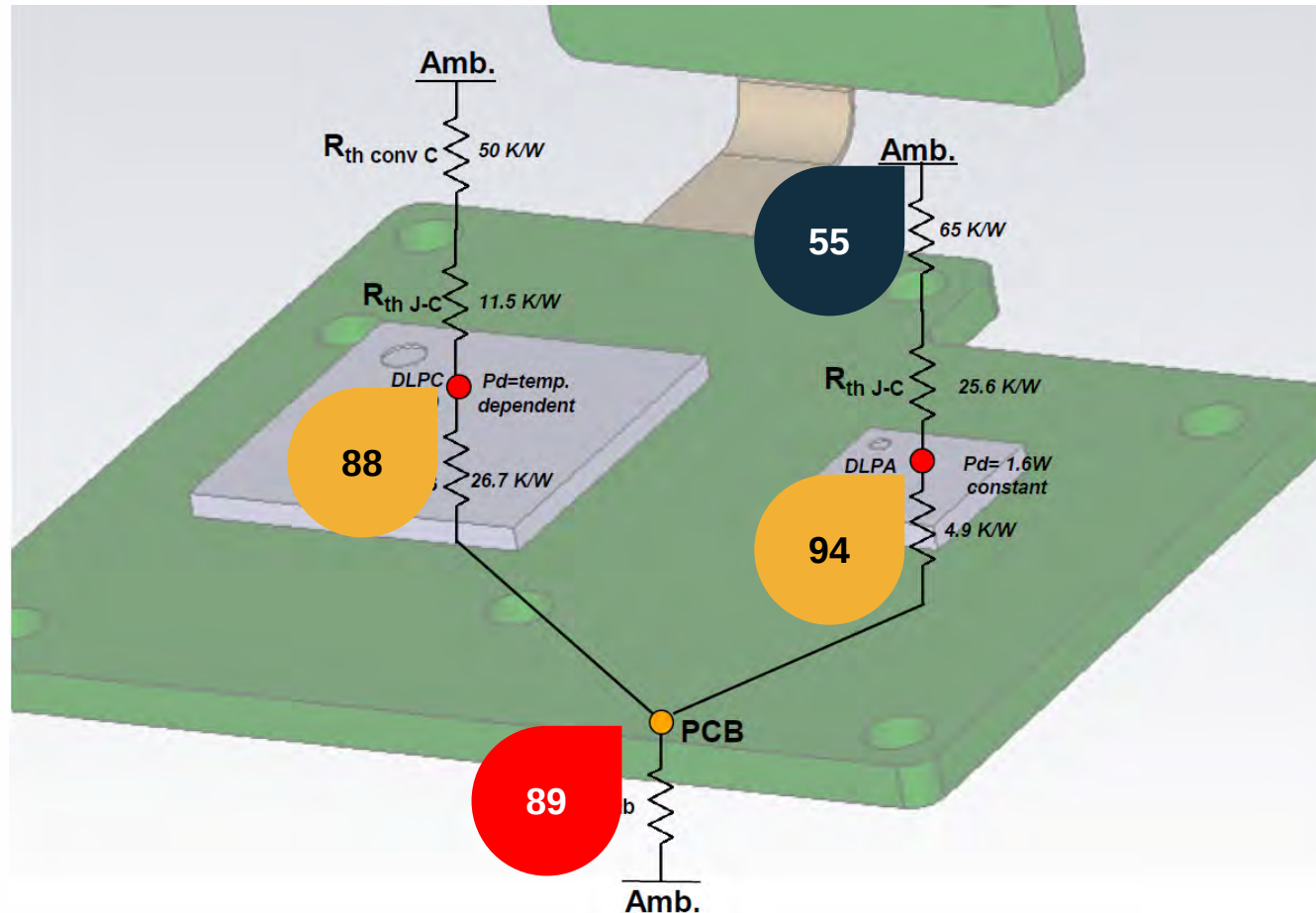


Figure 7 – Thermal Analysis results – improved. All temperatures in Celsius Degrees



Routing directives and strategy

- Signals routed on Layer 5
- Minimum number of VIAs: 2
- $Z_0 = 50\Omega$, $Z_{diff} = 100\Omega$

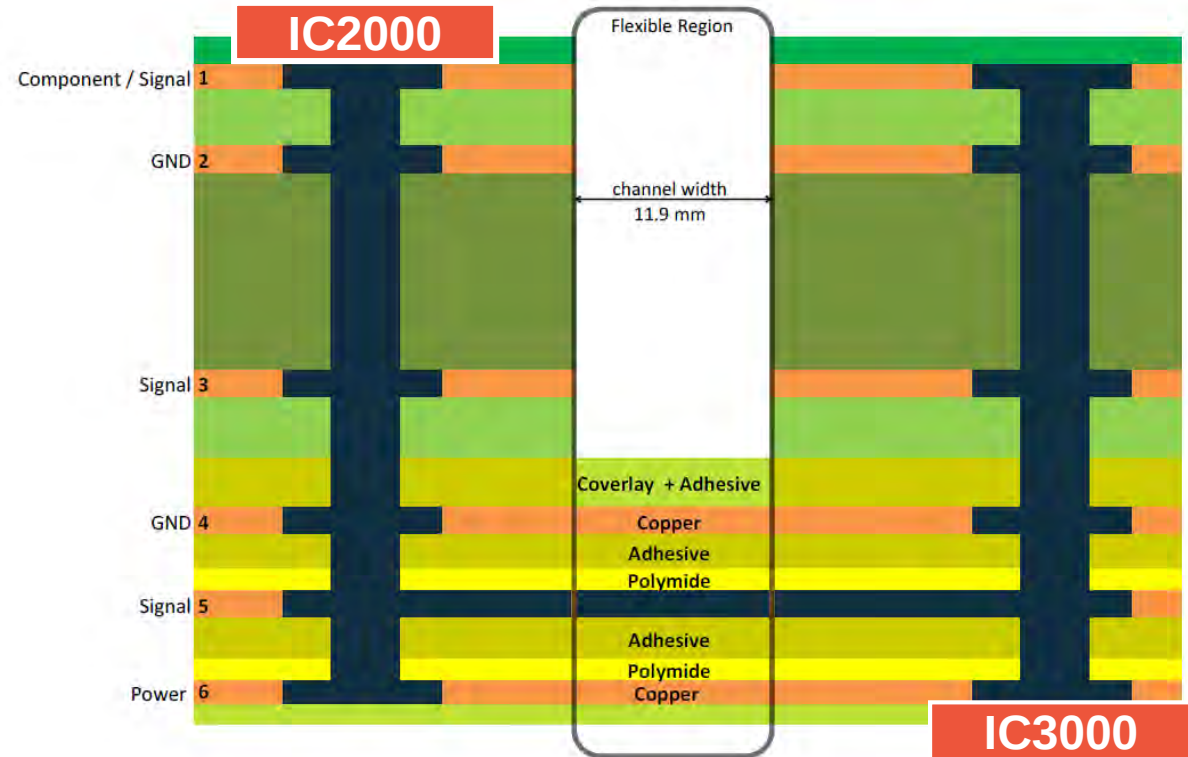


Figure 8 – Routing strategy for Sub-LVDS channel

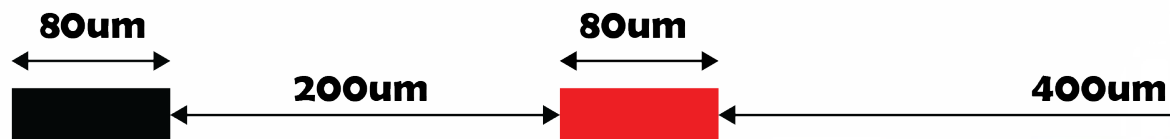


Figure 9 – Trace width and spacing for Sub-LVDS channel routed exclusively on Layer 5

Differential VIA design pattern

Via Characteristics

Drill Hole Diameter: **0.2 mm**

Ref Plane Opening H: **0.55 mm**

Ref Plane Opening W: **0.55 mm**

Via Spacing: **1 mm**

Baud Rate: **1.2 Gbaud**

Anisotropy of Material: **18 %**

Maximum Stub Length: **5.803 mm**

Odd Mode Impedance: **44.895 Ohms**

Differential Impedance: **89.790 Ohms**

Er Effective: **9.386**

Options

Base Copper Weight: ☒ 9um ☐ 18um ☐ 35um ☐ 53um ☐ 70um ☐ 88um ☐ 106um ☐ 142um ☐ 178um

Plating Thickness: ☐ Bare PCB ☐ 18um ☒ 35um ☐ 53um ☐ 70um ☐ 88um ☐ 106um

Property Selection: ☐ Via Properties ☒ Differential Vias

Layer Set: ☐ 2 Layer ☒ Multi Layer ☐ Microvia

Units: ☐ Imperial ☒ Metric

Substrate Options: Material Selection: **FR-4 STD**

Er: **3.8** Tg (°C): **130**

Temp Rise (°C): **20**

Temp in (°F): **36.0**

Ambient Temp (°C): **22**

Temp in (°F): **71.6**

Print Solve!

Information

Power Dissipation (dBm): **7.9331 dBm**

Via Thermal Resistance: **179.3 °C/W**

Via Count: **10**

Via Temperature: **17.9 °C/W per via**

Via Voltage Drop: **3.0838 mV**

Aspect Ratio 6.20:1

Temp in (°C): **42.0**

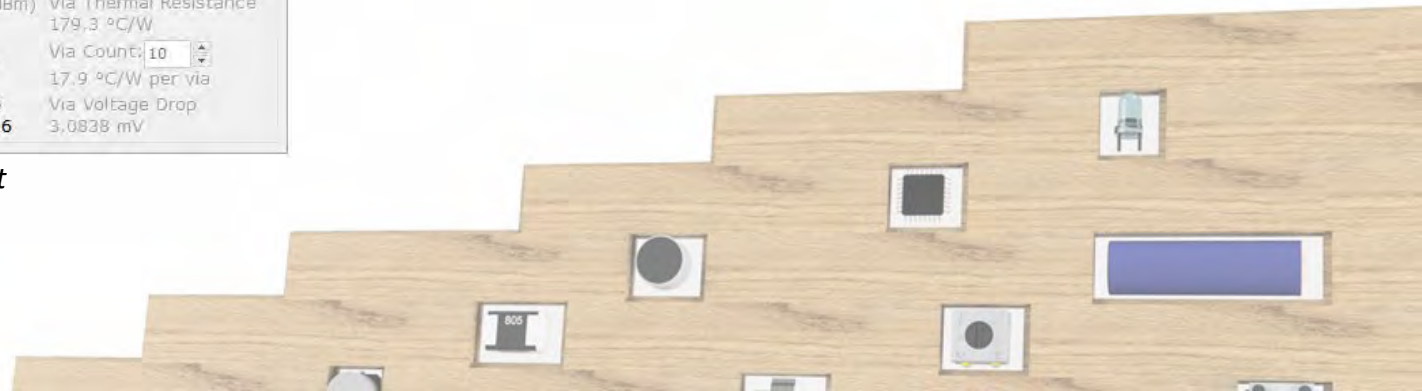
Temp in (°F): **107.6**

SATURN PCB DESIGN, INC
Turnkey Electronic Engineering Solutions

Follow Us:    

- “The Poor Man’s PCB Via Modeling Methodology” by Bert Simonovich
- $Z_{diffVIA} = 90 \Omega$

Figure 10 – Differential VIA design pattern – extract from SATURN PCB Toolkit



Intra-pair skew, in-pair skew, maximum etch length

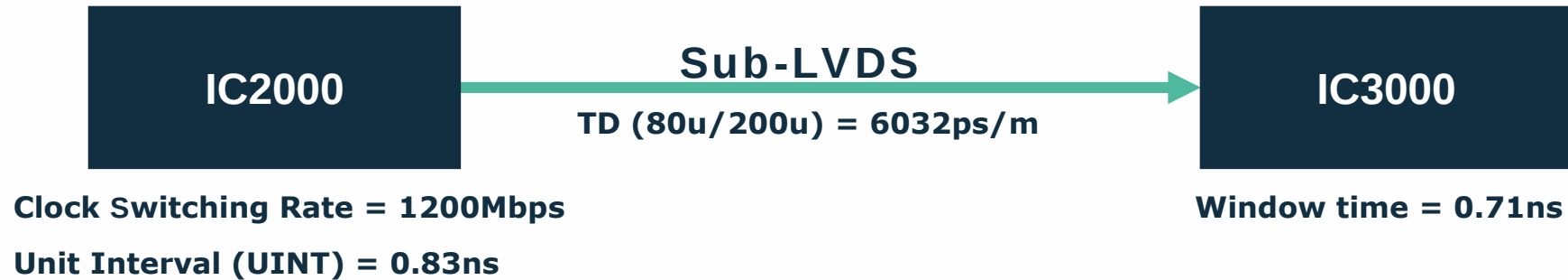


Figure 11 – Timing constraints IC2000, IC3000

- Intra-pair skew = $10\% * (0.83-0.71)\text{ns} = 0.012\text{ns}$
- In-pair skew = $5\% * (0.83-0.71)\text{ns} = 0.006\text{ns}$
- Maximum etch length = $40\% * 0.83\text{ns} = 0.332\text{ns}$



Routing the Sub-LVDS lines

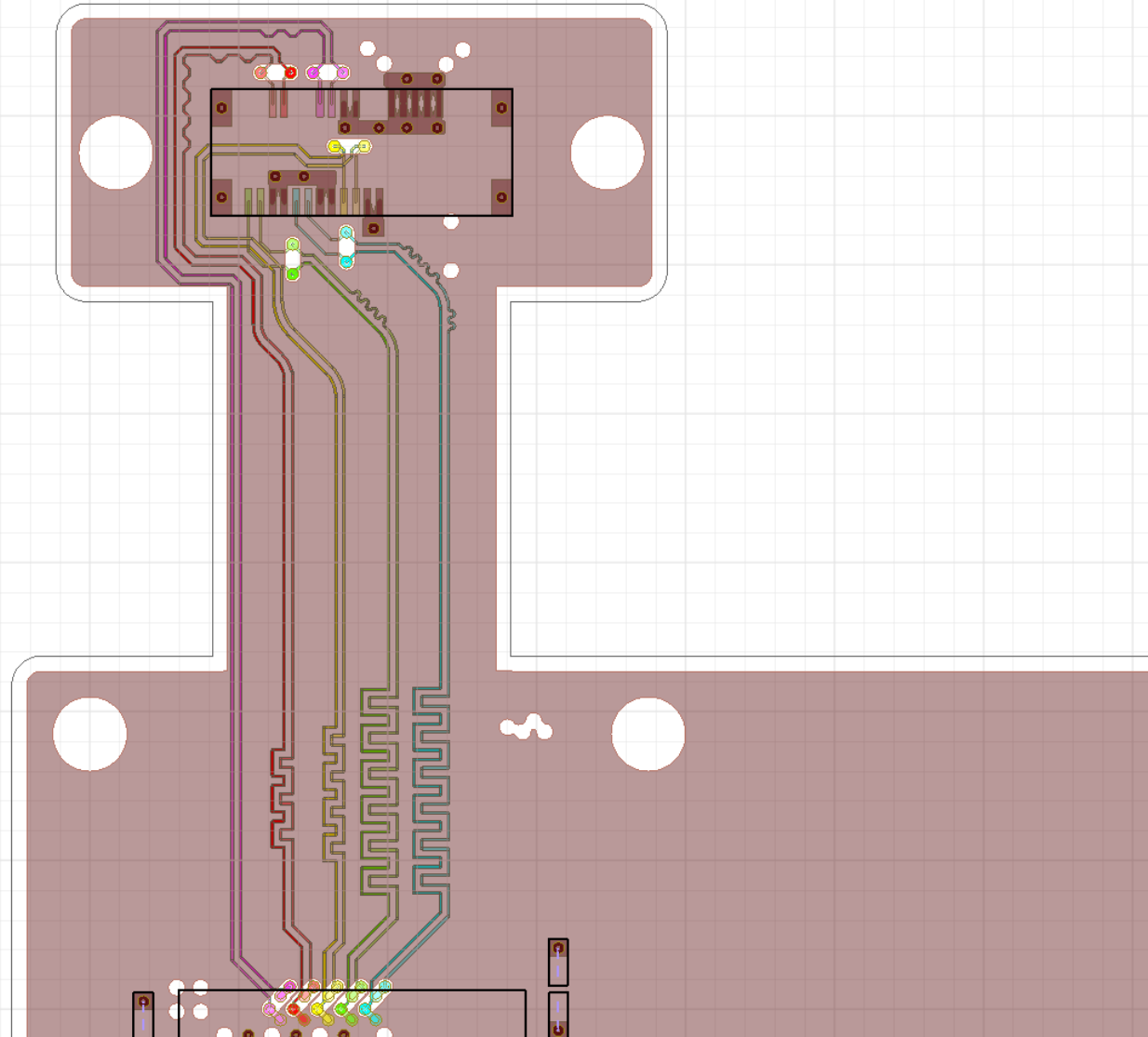


Figure 12 – Routed Sub-LVDS lines from IC2000 to IC3000

Evaluating Signal Quality – eye mask definition at IC3000

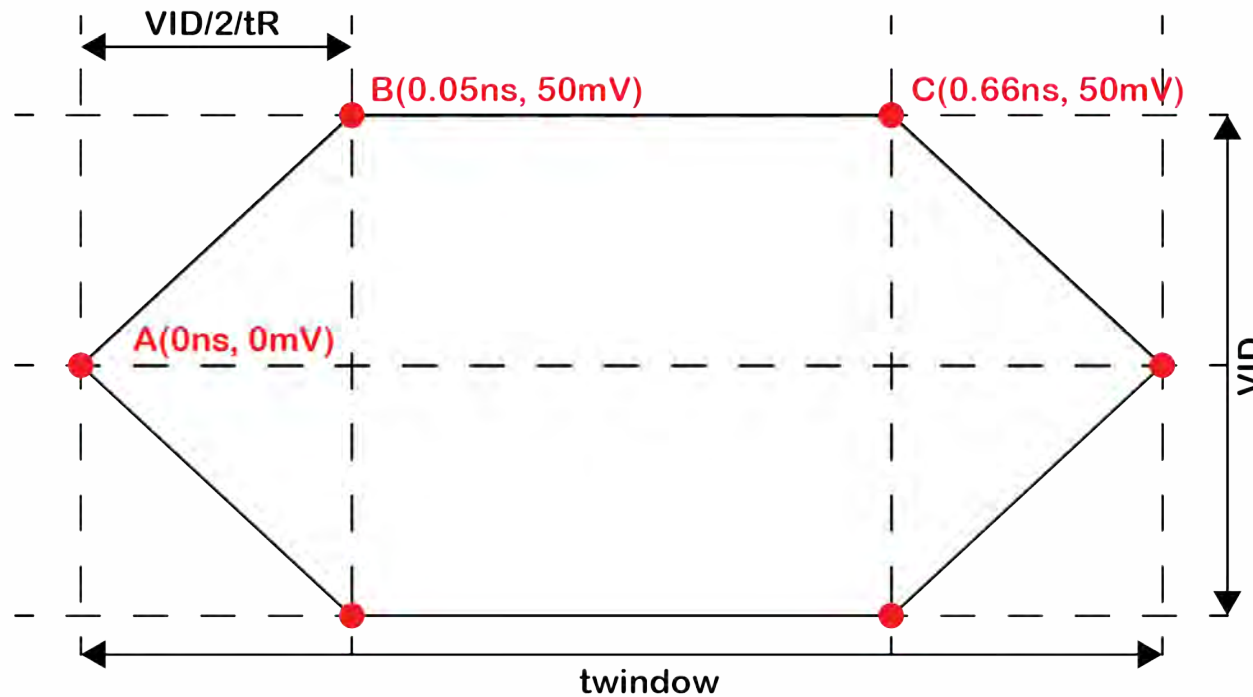
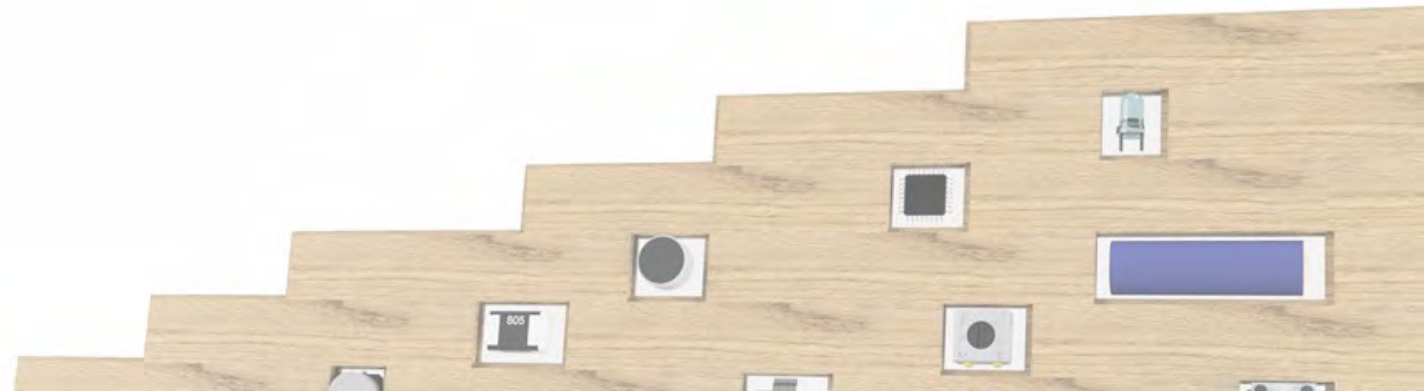


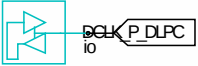
Figure 13 – Eye mask definition for DCLK, D0-D3

- Rise time = 1V/ns (worst case)
- Window time = 0.71ns
- Sub-LVDS differential voltage = **100mV**

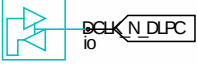


Evaluating Signal Quality – ANSYS Electronics Desktop Setup

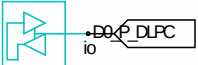
three_state
ID=1807
pin_name=A7



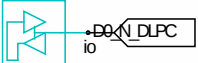
three_state
ID=1986
pin_name=B7



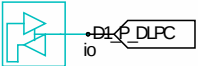
three_state
ID=1960
pin_name=A6



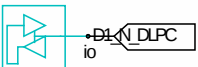
three_state
ID=1961
pin_name=B6



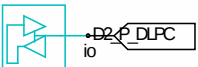
three_state
ID=1962
pin_name=A5



three_state
ID=1963
pin_name=B5



three_state
ID=1964
pin_name=A9



three_state



Design Properties
BPS = 1200MHz
trise = 250ps
tfall = 250ps
Rterm = 100ohm
dcdval = 0.06

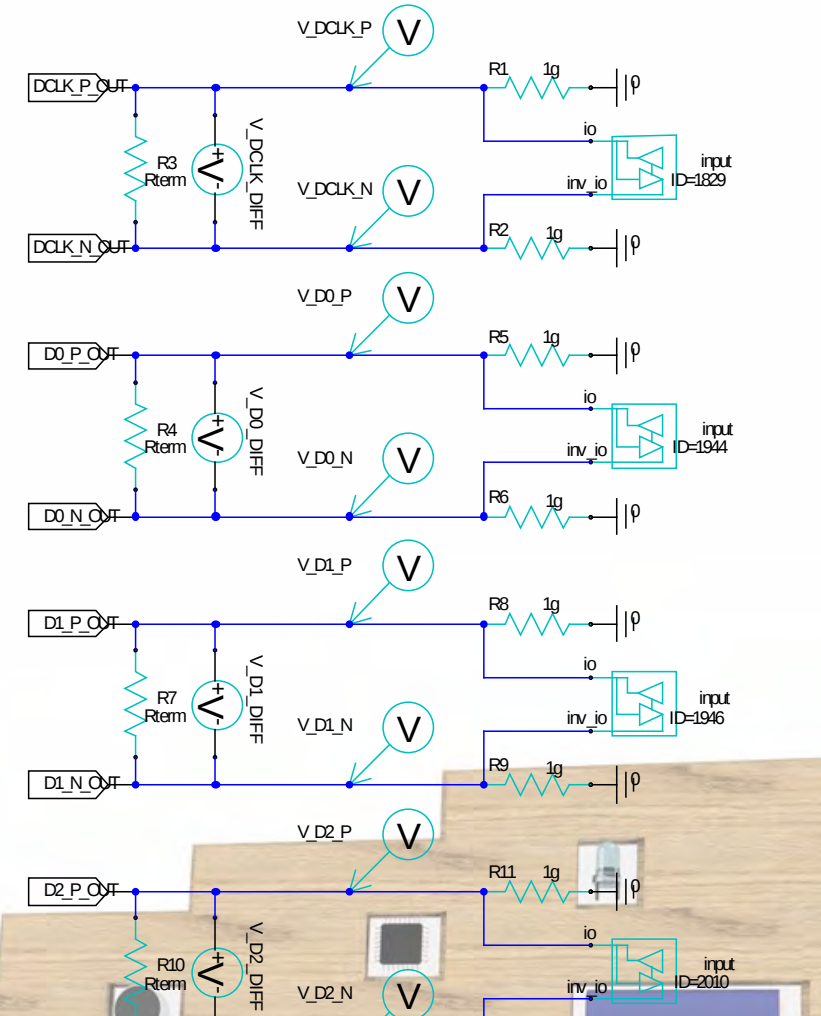
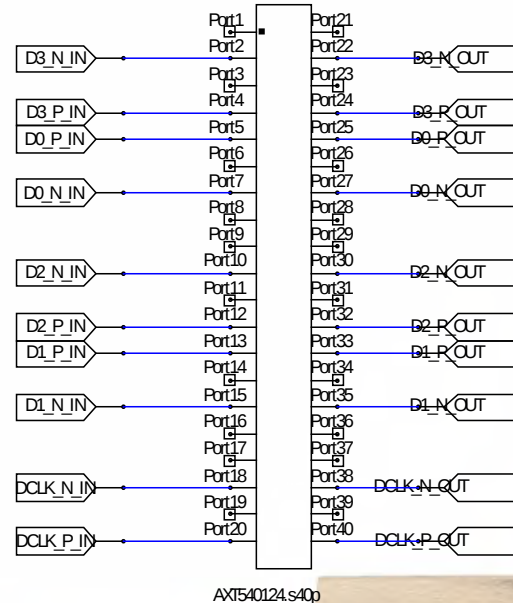
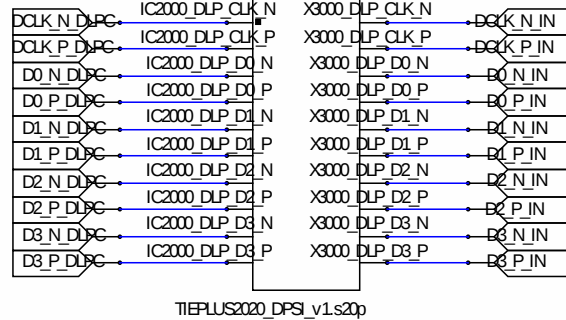
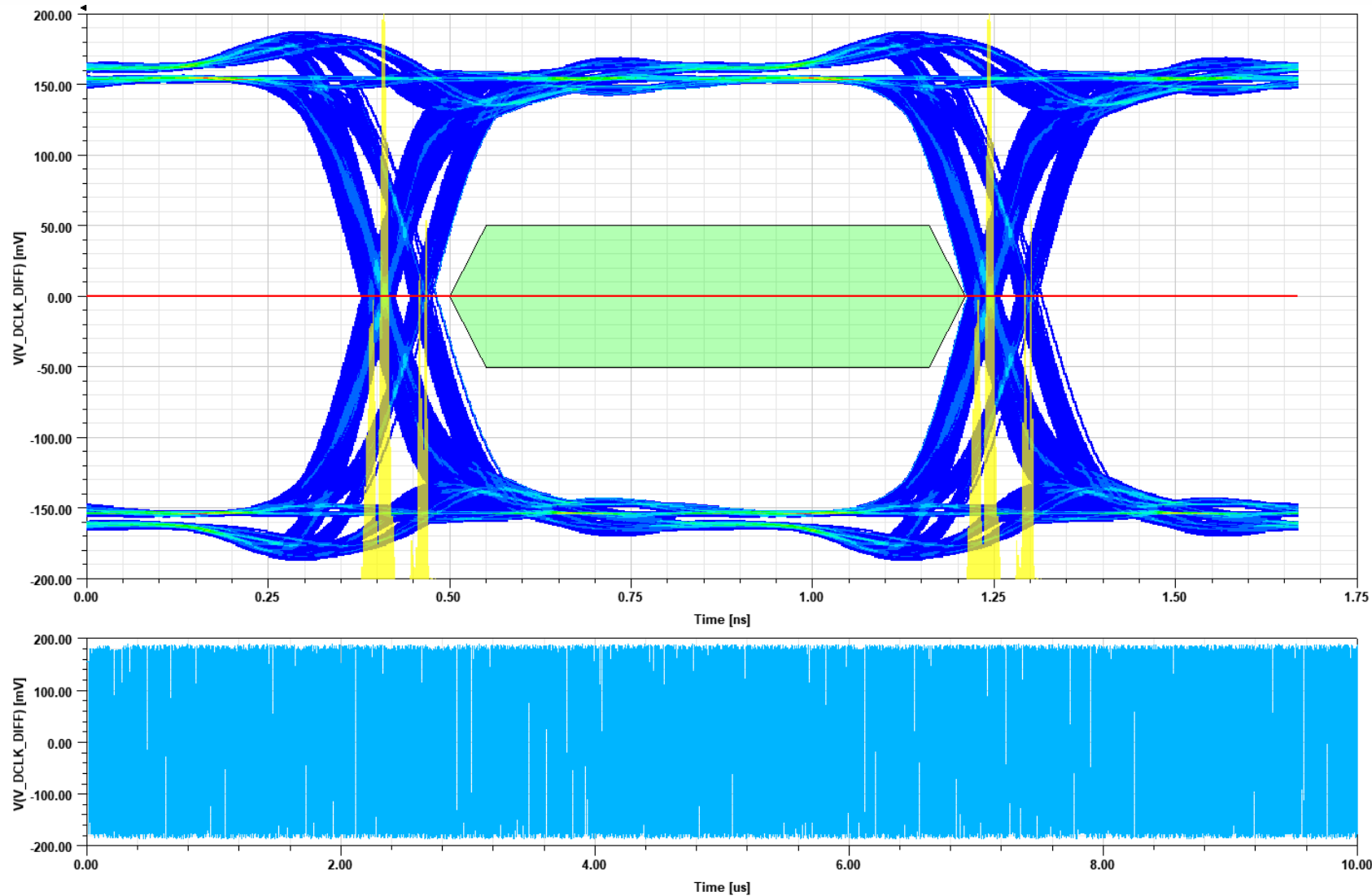


Figure 14 – ANSYS Electronics Desktop Setup, post-layout

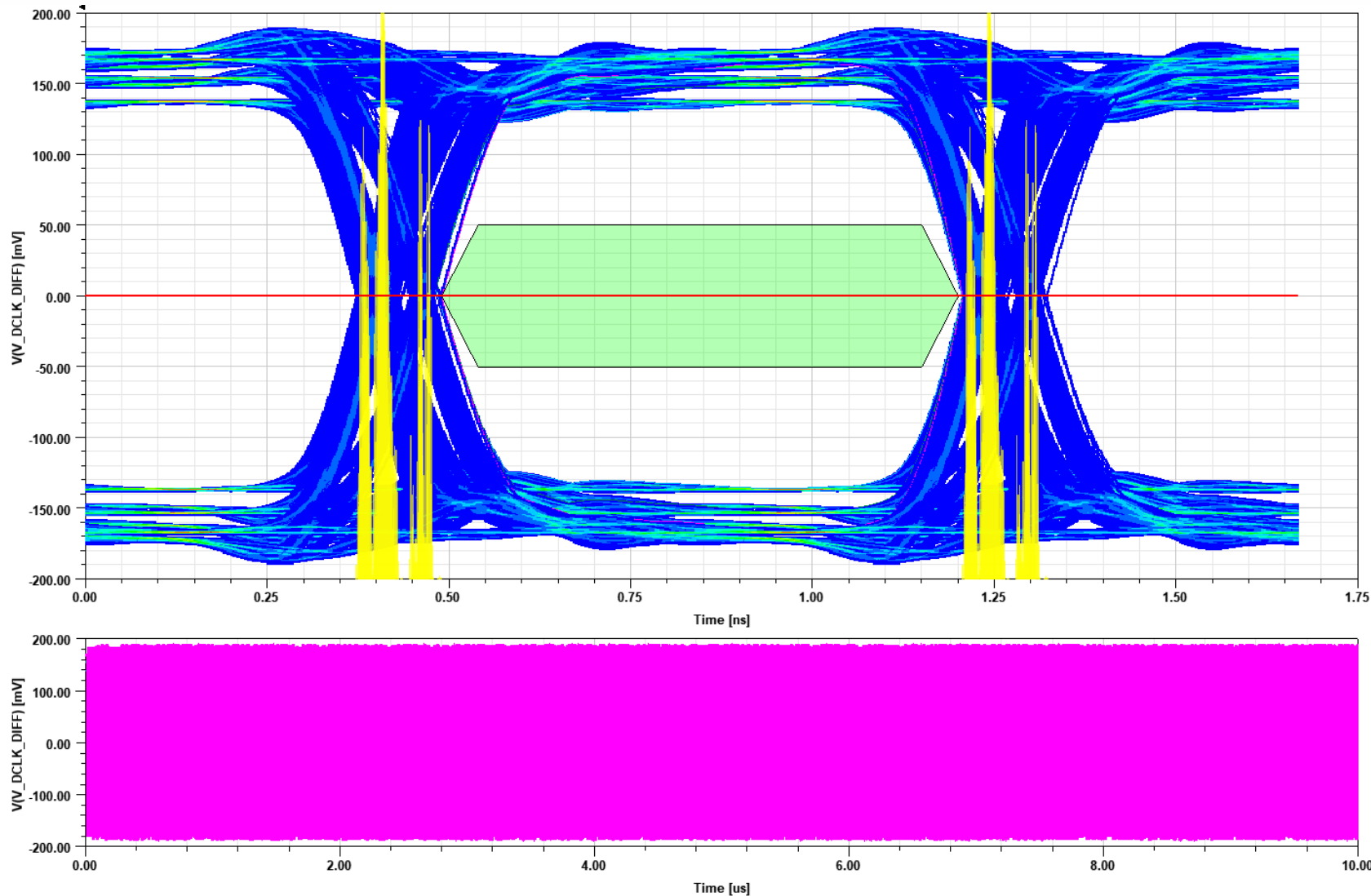
Evaluating Signal Quality – Eye diagram(s)



- IBIS type = SLOW

Figure 15 – Eye diagram for DCLK signal. 10us simulation time – 12048bits

Evaluating Signal Quality – Eye diagram(s)



- IBIS type = MIN
- Termination R swept from 80 to 120Ω

Figure 16 – Eye diagram for DCLK signal. 10us simulation time – 12048bits

Pre-layout characterization of PDN elements

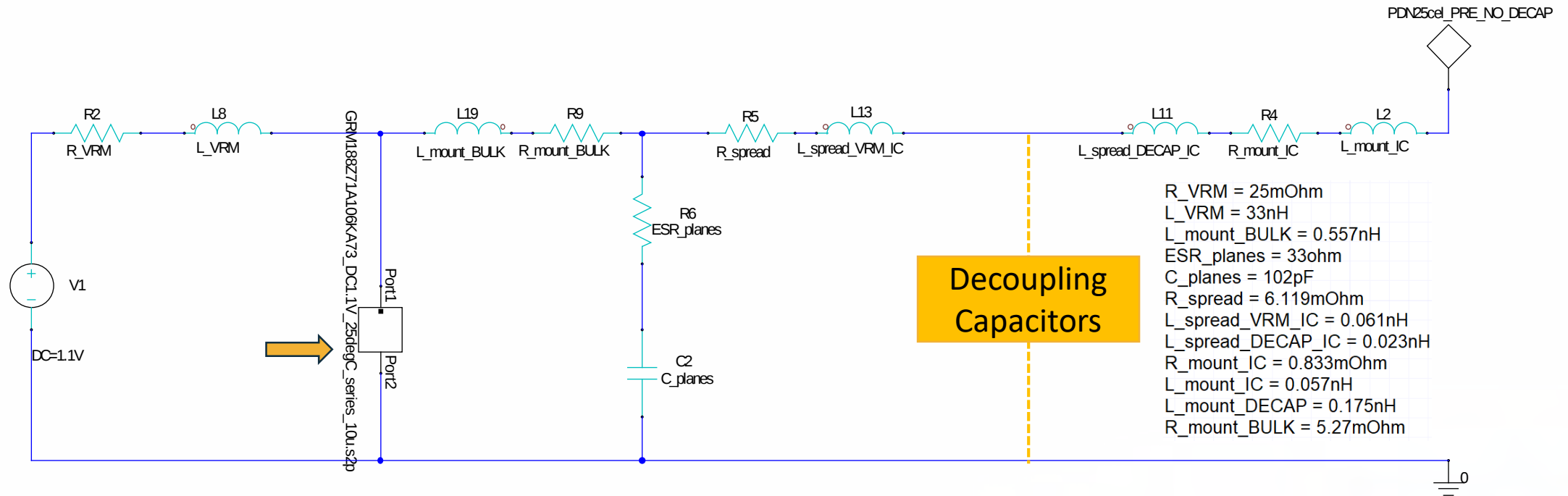
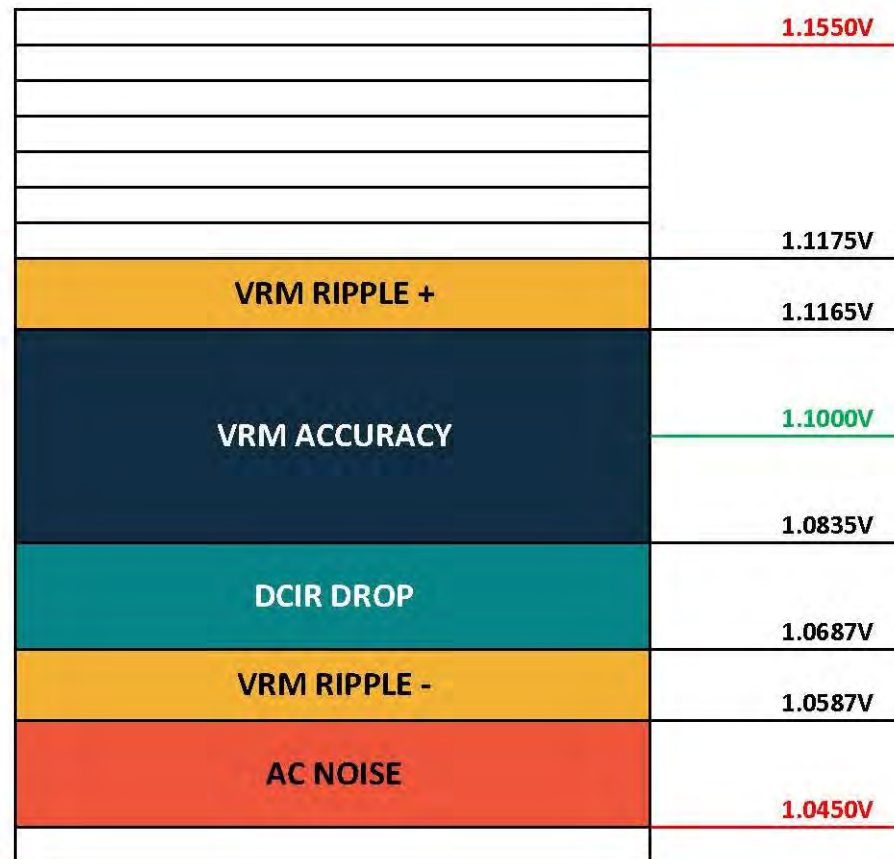


Figure 17 – Pre-layout characterization of PDN elements, only one 10uF bulk capacitor included. T capacitors = 25C.

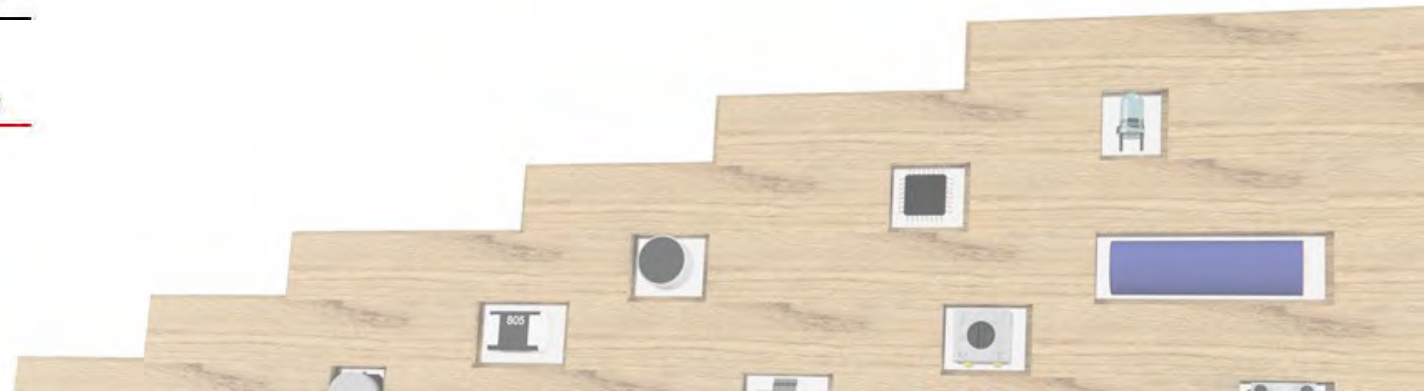
- Total DC resistance = $25 + 5.27 + 6.12 + 0.83\text{m}\Omega = \mathbf{37.22\text{m}\Omega}$

AC and DC noise budget



- $DCIR\ drop = (I_{leak} + I_{dyn}) * DC\ resistance$
 $= 0.39A * 37.22m\Omega = \mathbf{0.0147V}$
- $Z\ target = 0.01376V / 0.196A = \mathbf{70m\Omega}$

Figure 18 – AC and DC noise budget



Impedance profile from the IC's perspective

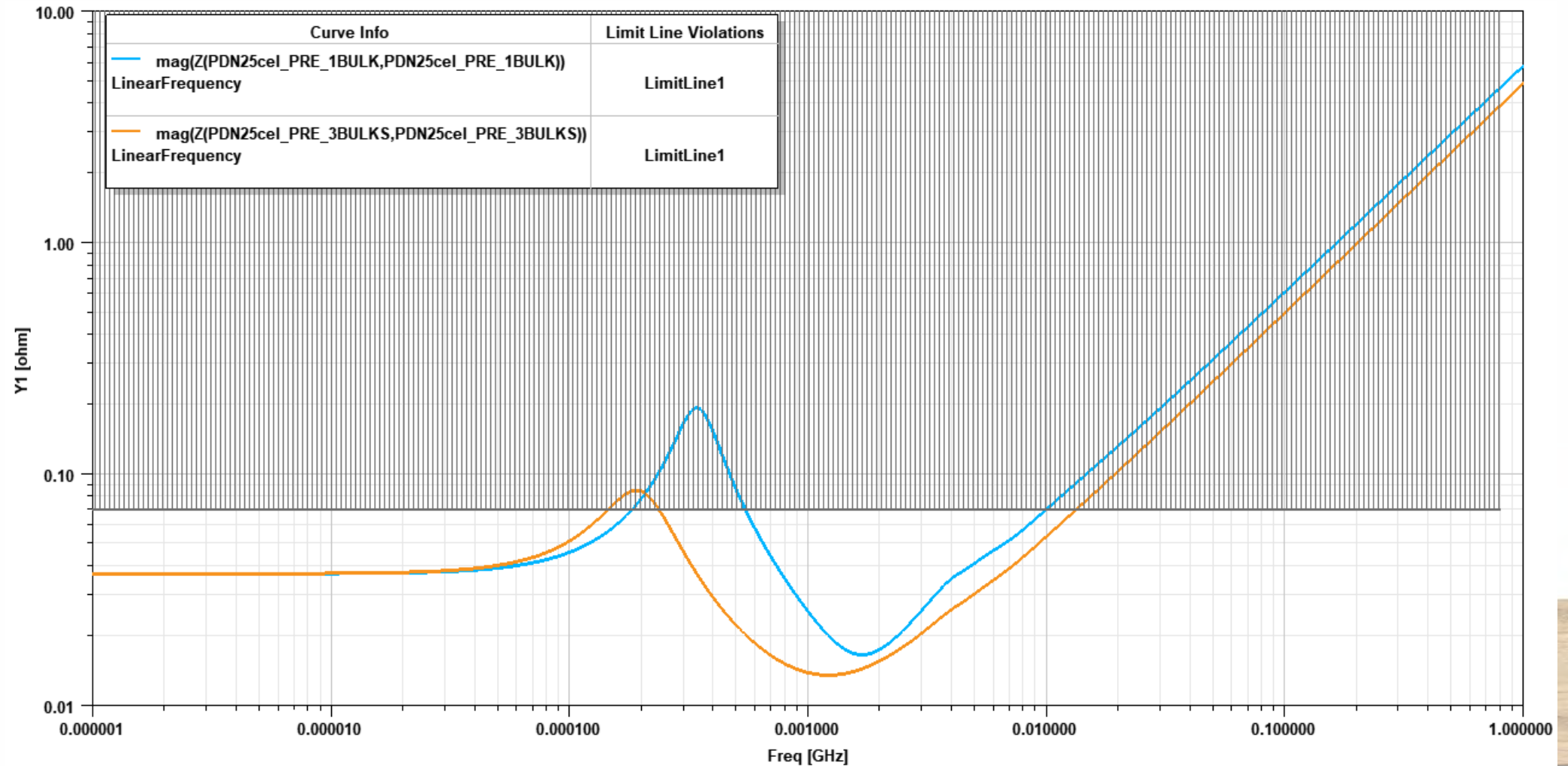


Figure 19 – Impedance profile from the IC's perspective.
1 vs 3 bulk capacitors, no decoupling. T capacitors = 25C.

Pre-layout characterization of PDN elements

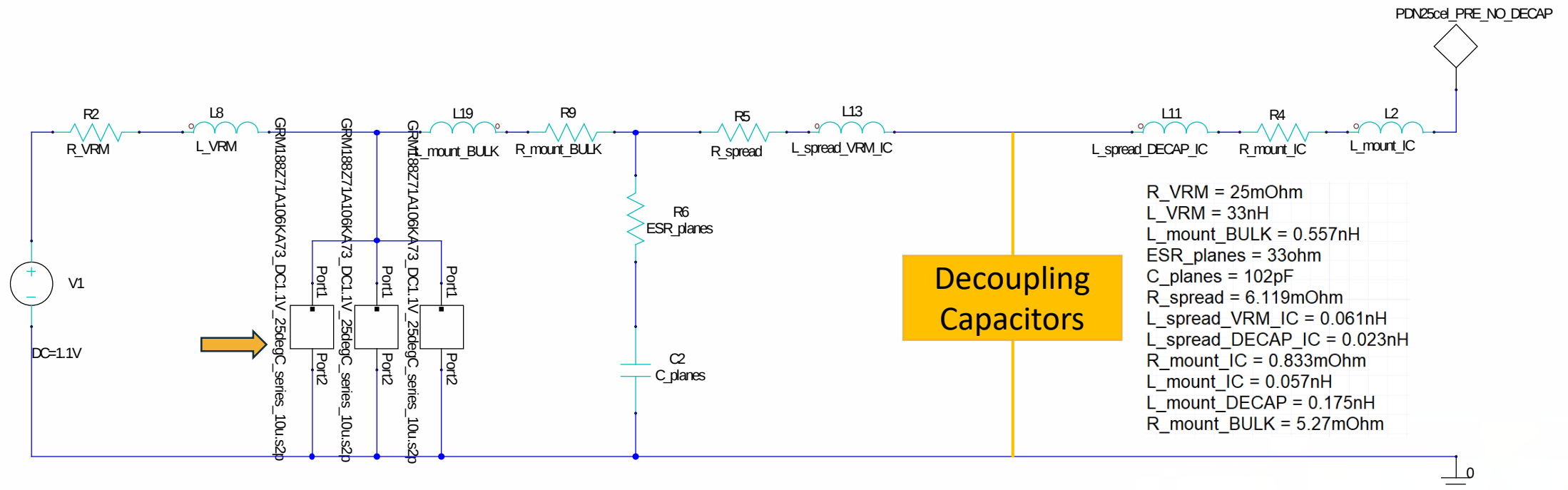
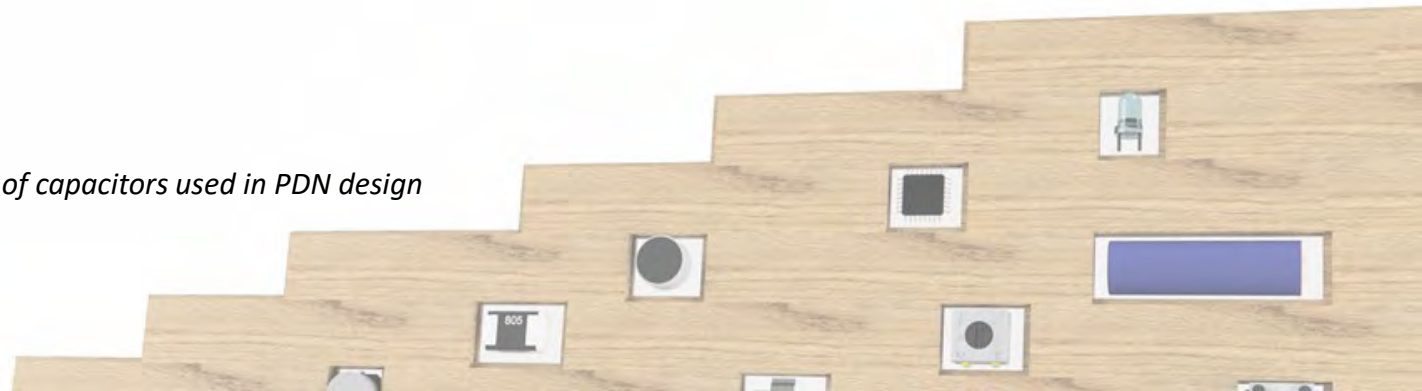


Figure 20 – Pre-layout characterization of PDN elements, three 10uF bulk and 5 decoupling capacitors included. T capacitors = 25C.

Ref. Des.	Value	MURATA Part. No.
C26, C27, C28	10 μ F	GRM188Z71A106KA73
C2001	2200nF	GRM155Z71A225KE01
C2002	1000nF	GRT155C71A105KE13
C2003	470nF	GRT155R71A474KE01
C2004	220nF	GRT155R71A224KE01
C2005	100nF	GCH155R71A104KE01

Table 1 – List of capacitors used in PDN design



5 Power Integrity – pre-layout

Impedance profile from the IC's perspective

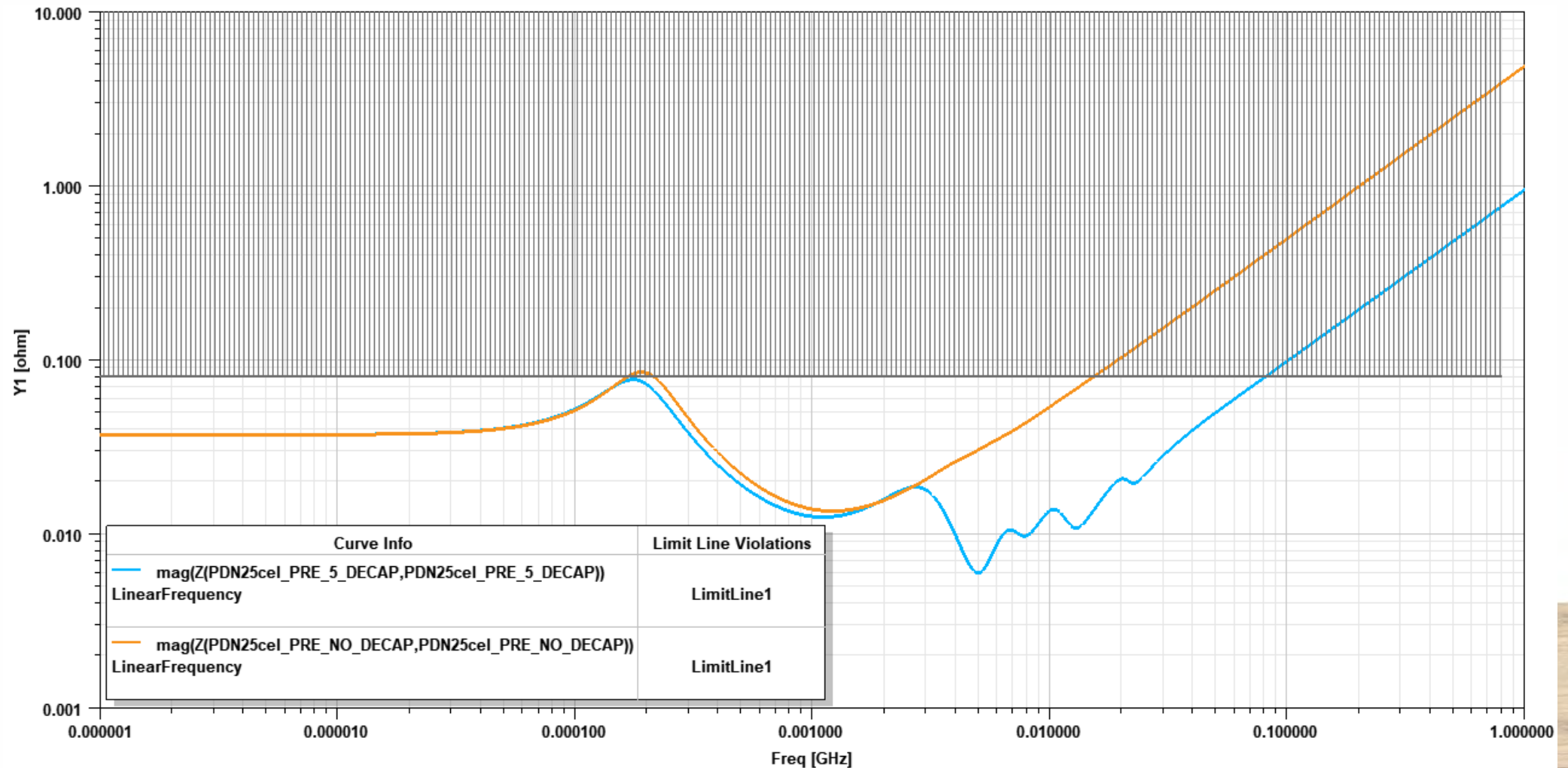


Figure 21 – Impedance profile from the IC's perspective.
3 bulk and 5 decoupling capacitors vs only 3 bulk. T capacitors = 25C.

Impedance profile from the IC's perspective

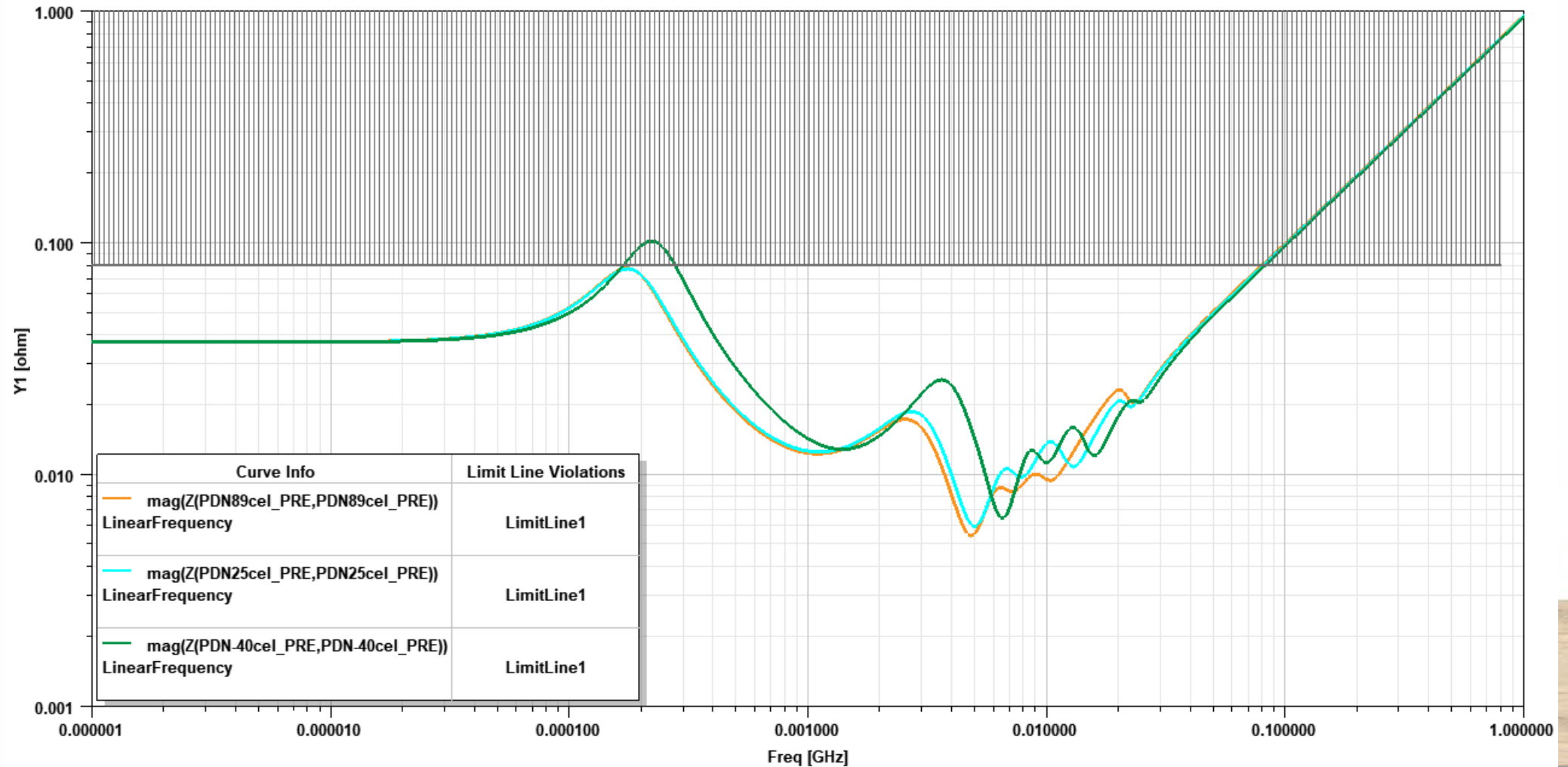


Figure 22 – Impedance profile from the IC's perspective.
3 bulk and 5 decoupling capacitors. T capacitors = -40C, 25C, 89C.

Post-layout parasitic extraction of PDN elements

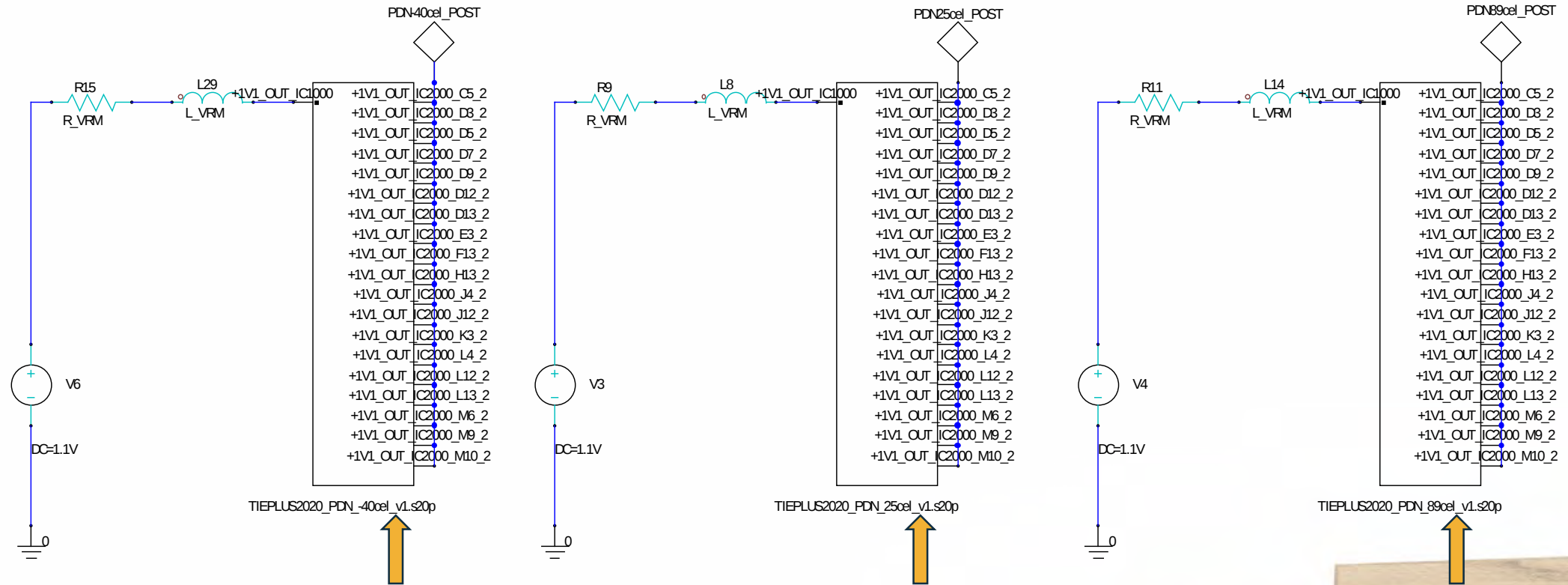


Figure 23 – Post-layout parasitic extraction of PDN elements, at three different temperatures: -40C, 25C and 89C

Impedance profile from the IC's perspective

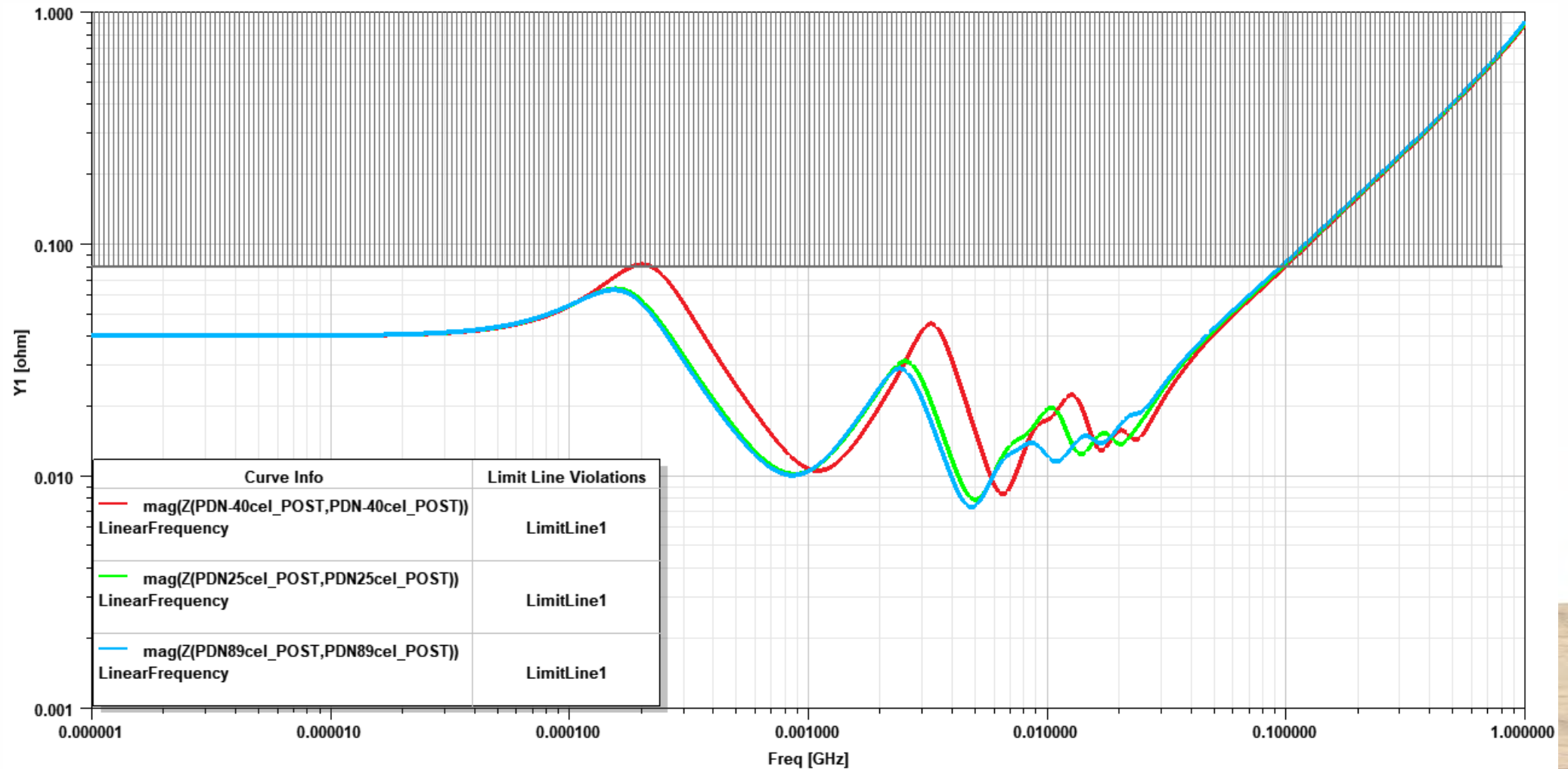


Figure 24 – Impedance profile from the IC's perspective, parasitic elements extracted at three different temperatures: -40C, 25C and 89C

- Thermal, Signal and Power integrity issues were addressed
- Simple analytical approximations provided a viable pre-layout analysis model
- Not all interface timing issues were addressed
- Routing could be improved for Sub-LVDS lines
- No PI analysis was performed for the 1V8 rail
- PDN for 1V1 and 1V8 rails under the BGA could be improved



Thank you for your attention!

