TIEplus 2020 Technical Report - Picture Generation Unit (PGU) Thermal, Signal and Power Integrity Analysis

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October 13, 2020

Introduction

This technical report presents the simulation results, pre-layout and post-layout analysis for the Picture Generation Unit (PGU). The fields investigated are as requested in the description of the project, signal and power integrity and thermal aspects. For the pre-layout analysis Polar SI9000 2D extractor was used to define single and differential impedance guidelines based on the given stackup and Saturn PCB Toolkit was used to define a differential VIA design pattern. Also in the pre-layout analysis Matlab was used to quickly solve the equations describing the equivalent thermal circuit of the board and circuits system. The layout was developed using Orcad Capture CIS and Cadence Allegro PCB Designer v16.6 2014. This posed some issues since to the best of my knowledge this version does not perform oval cutouts in the power planes around differential pairs. Post-layout analysis were performed in Ansys Siwave and results exported as Touchstone files. Simulation capacitors models from Murata were used. As a circuit simulator, Nexxim from Ansys Electronics Desktop (AEDT) was used for both pre and post-layout simulations.

1 Thermal Analysis

First part of this investigation is the thermal one since $I_{leakage}$ for DLPC2020 which is a mandatory quantity in the next stages of investigation is temperature-dependent. A thermal resistances model as described in slide 9/10 of the TIEPLUS2020 subject was the starting point of this part of analysis. Unfortunately, even if far more precisely would have been a CFD approach, given the time constraints, it was beyond the scope of this investigation.

Several simplifications were made in the thermal model of the PCB, as mentioned in the initial requirements of the project. The ambient temperature, T_a, was considered constant on both the TOP and BOTTOM parts which may not be exactly right since the board is standing horizontally and a temperature gradient for the ambient could appear. Secondly, the PCB temperature, T_{PCB}, was considered constant in the X,Y and Z directions of the board, which once again is not a right assumption to be made. In accordance with the copper fraction in

the board and layers thicknesses, an equivalent thermal conductivity (or resistivity) could have been approximated and two additional thermal resistances could have been included in the model, one for the planar XY propagation and one for the vertical Z direction.

The only thermal resistance unknown in the model provided in slide 9/10 of the project description was the $R_{thPCBamb}$, which is solely a natural convection resistance since no other cooling method is used. I divided this resistance in two parallel ones,$R_{thPCBamb(T)}$ and $R_{thPCBamb(B)}$, one for the TOP and one for the BOTTOM part of the PCB since I considered different convection coefficients, h_{TOP} and h_{BOTTOM} for the TOP and BOTTOM areas. Moreover, the TOP area is slightly smaller than the BOTTOM one (convention from the PCB does not take place in the small areas occupied by IC1000 and IC2000). In parallel with these two thermal resistance there is also a third one, $R_{thrad(T+B)}$ describing the radiation heat transfer which should have been omitted in this investigation but however it was not (will later be discussed why).

Equations 1 and 2 were used to calculate the thermal resistances of convection for the TOP and BOTTOM surfaces of the PCB. The convection coefficients are still function of an unknown variable, T_{PCB}.

$$\begin{cases} R_{thPCBamb(T)} = \dfrac{1}{h_{TOP} \cdot A_{TOP}} \\ R_{thPCBamb(B)} = \dfrac{1}{h_{BOTTOM} \cdot A_{BOTTOM}} \end{cases} \tag{1}$$

$$\begin{cases} h_{TOP} = 1.6 \cdot (T_{PCB} - T_a)^{\frac{1}{3}} \\ h_{BOTTOM} = 0.65 \cdot \left(\dfrac{T_{PCB} - T_a}{A_{BOTTOM}/P} \right)^{\frac{1}{4}} \end{cases} \tag{2}$$

Based on the calculated thermal resistances of convection from the PCB to ambient and the provided values for all the other thermal resistances involved, the equivalent circuit from Figure 1 was developed. Based on this schematic, Equations 3 were developed with 5 unknown values: T_{jDLPA}, T_{jDLPC}, T_{PCB}, $P_{D1(A)}$ and $P_{D1(C)}$. $P_{D(A)}$ is fixed at 1.6W and $P_{D(C)}$ can be estimated based on an initial assumption about the junction temperature of DLPC2020. After the equation system is resolved, the $P_{D(C)}$ can be once again better estimated based on the obtained value for T_{JDLPC}. This is actually how I solved the system, in an iterative way using Matlab for all the tedious calculations.

Since h_{TOP} and h_{BOTTM} are a function of T_{PCB}, this temperature also had to be initially assumed and later at a second iteration corrected with the one obtained from a previous step. This is mainly the reason for using an automated way as a Matlab script to solve these equations.

I should mention that $R_{thPCBamb}$ is formed by the TOP and BOTTOM convection thermal resistance in parallel with a radiation thermal resistance, $R_{thrad(T+B)}$. Firstly in this stage of the analysis, radiation was omitted (reason why in Figure 1 $R_{thrad(T+B)}$ is disabled). The results from Equations 3 are displayed in Table 1.

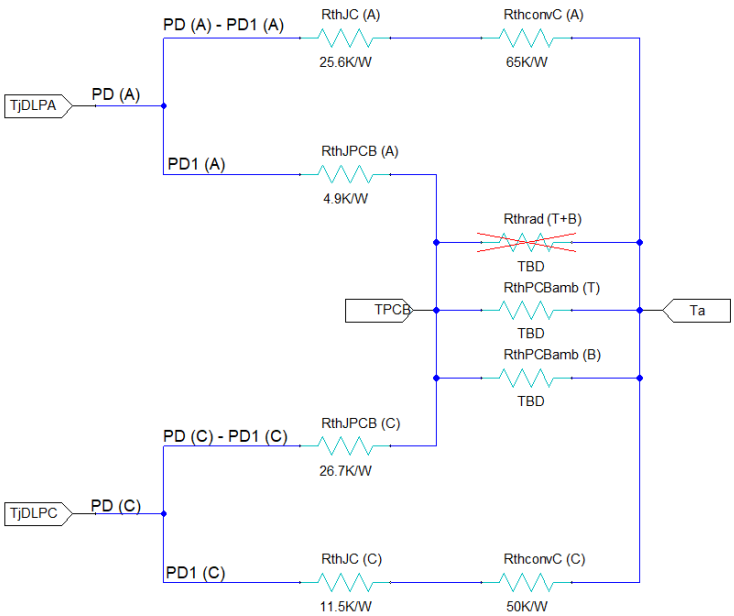


Figure 1: Equivalent thermal resistances circuit used for thermal modeling. Radiation is at first neglected from analysis.

$$\begin{cases} T_{jDLPA} - T_a = P_{D1(A)} \cdot [R_{thJC(A)} + R_{thconvC(A)}] \\ T_{jDLPA} - T_{PCB} = [P_{D(A)} - P_{D1(A)}] \cdot R_{thjPCB(A)} \\ T_{jDLPC} - T_a = P_{D1(C)} \cdot [R_{thJC(C)} + R_{thconvC(C)}] \\ T_{jDLPC} - T_{PCB} = [P_{D(C)} - P_{D1(C)}] \cdot R_{thjPCB(C)} \\ T_{PCB} - T_a = [P_{D(A)} - P_{D1(A)} + P_{D(C)} - P_{D1(C)}] \cdot R_{thPCBamb} \end{cases} \tag{3}$$

Observing the results from Table 1 and comparing junction temperatures for DLPC2020 and DLPA2020 with the maximum rating from their datasheets I conclude that the maximum recommended values for junction temperature are not violated for neither of the two ICs.

Table 1: Values resulted from solving Equations3 without taking into account radiation.

Quantity	Value	Unit
h_{TOP}	5.18	$W/(K \cdot m^2)$
$R_{thPCBamb(T)}$	160.09	K/W
h_{BOTTOM}	5.04	$W/(K \cdot m^2)$
$R_{thPCBamb(B)}$	140.12	K/W
$R_{thPCBamb}$	74.72	K/W
T_{jDLPA}	113.01	$°C$
T_{jDLPC}	101.73	$°C$
T_{PCB}	108.30	$°C$

Table 2: Values resulted from solving Equations 3 when radiation is taking into consideration with an emissivity of 0.8.

Quantity	Value	Unit
h_{TOP}	5.18	$W/(K \cdot m^2)$
$R_{thPCBamb(T)}$	160.09	K/W
h_{BOTTOM}	5.04	$W/(K \cdot m^2)$
$R_{thPCBamb(B)}$	140.12	K/W
$\alpha_{radiation}$	7.47	$W/(K \cdot m^2)$
$R_{thrad(T+B)}$	51.04	K/W
$R_{thPCBamb}$	30.27	K/W
T_{jDLPA}	94.92	$°C$
T_{jDLPC}	88.44	$°C$
T_{PCB}	89.24	$°C$

However, due to the extremely large temperature obtained for the circuit board which is over $100°C$, I investigated a way to improve my thermal simulation model.

Radiation is an important aspect when investigating thermal aspects and should not be neglected in any analysis. Since no data about the emissivity of the PCB was provided, I approximated a 0.8 value for it. A thermal resistance based on radiation using Equation 4 was defined where $\alpha_{radiation}$ is calculated based on Equation 5.

$$R_{thrad} = \frac{1}{\alpha_{radiation} \cdot (A_{TOP} + A_{BOTTOM})} \tag{4}$$

$$\alpha_{radiation} = \varepsilon \cdot \sigma \cdot ({T_{PCB}}^2 + {T_a}^2) \cdot (T_{PCB} + T_a) \tag{5}$$

Once again the thermal circuit was resolved with iterations using Matlab and the final results are displayed in Table 2. All the temperatures involved are slightly lower but the most important figure of interest, T_{PCB} has dropped below $100°C$, at a value of $89°C$.

Even if temperature values from Table 2 are based on the assumption of an emissivity value not given in the initial project description, I used these values in the following stages of this work since the initial ones (resulted by ignoring the radiation mechanism) were too high.

2 Signal Integrity

2.1 Pre-Layout Analysis - routing directives

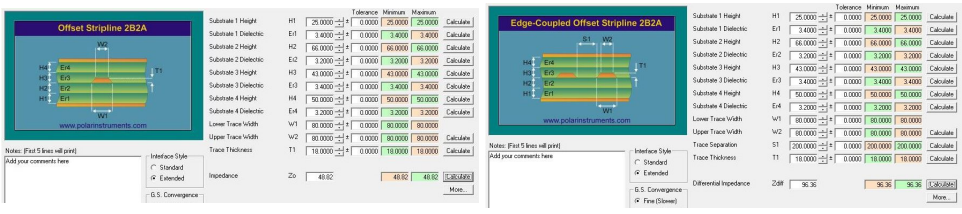
According to specifications, Sub-LVDS lines must be routed as 100Ω differential pairs with a single-ended Impedance of 50Ω. Based on the provided PCB stack-up, I investigated routing directives, trace width and spacing using Polar SI9000 2D Extractor. Since the only available

layer for signal on the flexible area was Layer5, I was forced to choose this layer for signal routing from DLPC2020 to X3000.

After configuring Polar SI9000 with the corresponding stack-up parameters I obtained a trace width of 80μm for a single-ended characteristic impedance of ≈50Ω as seen in Figure 2a. Going lower than this width would have violated the minimum trace width requirements. Moving to the differential impedance calculator, as seen in Figure 2b a spacing of 200μm between the differential pair traces was required to obtain a differential impedance of ≈100Ω.

Inter-pair spacing should be as large as possible to minimize crosstalk between pairs. A general rule of 5W should have been followed which translates into a spacing between pairs of 400μm. This spacing constrain or even more, around 1300μm, was met on the flexible area but near the BGA and the X3000 connector. However, in the pre-layout analysis performed in AEDT a pair to pair spacing of 250μm was used to simulate a worst case situation.

Layer transition should be kept to a minimum, ideally to zero if this would be possible. Since the DLPC2020 IC is located on the TOP side and the X3000 connector on the BOTTOM, the minimum number of layer transition will be used, precisely two (one for BGA fanout and one for the X3000 connector).



(a) $Z_0 \approx 50\Omega$ dimensions

(b) $Z_{diff} \approx 100\Omega$ dimensions

Figure 2: Trace dimensions for stripline configuration on Layer 5 used for routing the differential data and clock pairs obtained using Polar SI9000.

2.2 Pre-Layout Analysis - differential pair design

Matching the impedance of a differential VIA pair with a target value is not an easy task and requires some tedious calculations based on the vertical dielectric constant of the circuit board, capacitance and inductance of the VIA pair [5]. Alternatively, a simple ECAD model of different VIA structures based on the final stack-up can be quickly investigated using full wave solvers to determine the best geometry to be used.

The simplest way for an initial pre-layout analysis I could find was by using Bert Simonovich's design guide for Differential VIA pairs called by the author himself "The Poor Man's PCB Via Modeling Methodology" [5]. Thankfully, Saturn PCB Design Toolkit implemented this algorithm in the "VIA Properties" tab starting from version 7.11 and the only thing left to do was to find an optimum design by leveraging VIA spacing and reference plane opening.

In developing the differential VIA structure I was interested in a VIA spacing as small as possible (near the 0.8mm BGA pitch) to be able to easily fanout from the DLPC2020's balls to Layer5. The options from Figure 3 were finally used in the design. I should mention that to the best of my knowledge, allegro PCB Designer 16.6 2014 does not have an integrated option to automatically perform oval slots in the reference planes so I designed them manually in Siwave by some boolean subtraction.

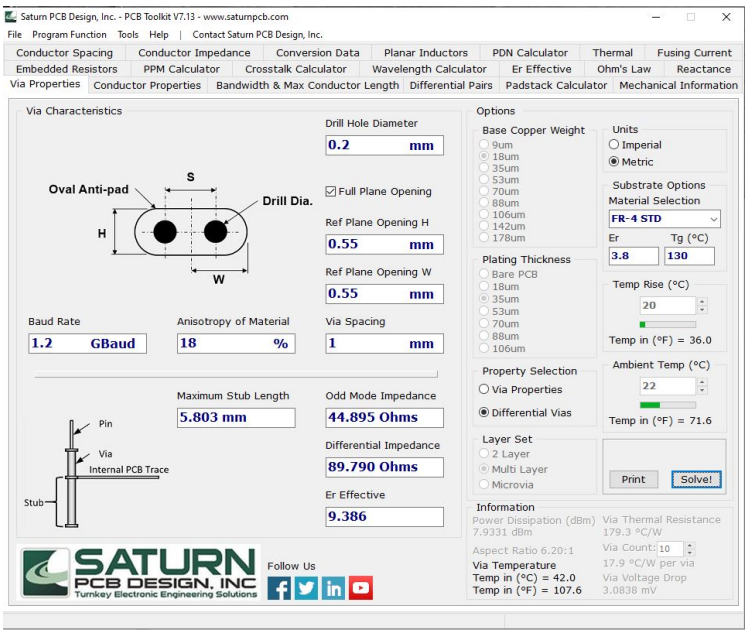


Figure 3: Differential VIA design using Satun PCB Design Toolkit. $Z_{diff} \approx 90\Omega$.

2.3 Pre-Layout Analysis - intra-pair skew

Also from Polar Si9000 2D (Figure 2) I extracted the time delay (**TD**) of this differential transmission line to be of **6.032ns/m**. The DLPC2020 IC clock switching rate of 1200Mbps translates in an Unit Interval (UINT) of **0.83ns**. Based on this value I estimated the total delay of the line not to be longer than 50% of the UINT as stated in Equation 6.

$$TD_{max} = 50\% \cdot UINT = 0.415ns -> Len_{max} = 68mm \tag{6}$$

With an UINT of 0.83ns and the minimum window time for DLP2020 of **0.71ns**, only **0.12ns** are available for any jitter, mismatch or any other timing signal degradation effect. This last value is the one I used as reference for the in-pair and intra-pair skew values as calculated in Equations 7.

$$\begin{cases} SKEW_{intra-pair} = 10\% \cdot 0.12ns = 0.012ns -> SKEW_{intra-pair} = 1989\mu m \\ SKEW_{in-pair} = 5\% \cdot 0.12ns = 0.006ns -> SKEW_{in-pair} = 994\mu m \end{cases} \tag{7}$$

2.4 Pre-Layout Analysis - circuit simulation

Using a pair of 5 Filed Solver Transmission Lines from Ansys Electronics Desktop's Libraries I configured a pre-layout analysis to verify channel compliance with the datasheets before starting to route the actual lines in accordance with the routing directives already discussed. I used a spacing between pairs of 250μm, a worst case situation which would not be the case on the actual ECAD board (exception are the isolated area near the X3000 connector and the DLPC2020).

The IBIS models provided in the project description were configured as output for DLPC2020 and as input for DLP2020. Between the two ICs there was the transmission line circuit element and also the Touchstone file for X3000. Termination resistors of 100Ω were included in the circuit because they are not internal to the IBIS models. A Pseudo Random Bit Sequence of $2^{18} - 1$ bits was generated with a UINT of 1/BPS, where BPS is the 1200Mbps bit rate. A total simulation time of 10μs generated a number of 12048bits.

The eye mask, visible also in Figure 4 was defined in accordance with DLP2020's specifications: the eye must have a minimum voltage of **VID = 100mV** and a minimum window duration of **0.71ns**. The other upper marginal points were calculated based on the rise time (highest value for the rise time giving the largest eye opening).

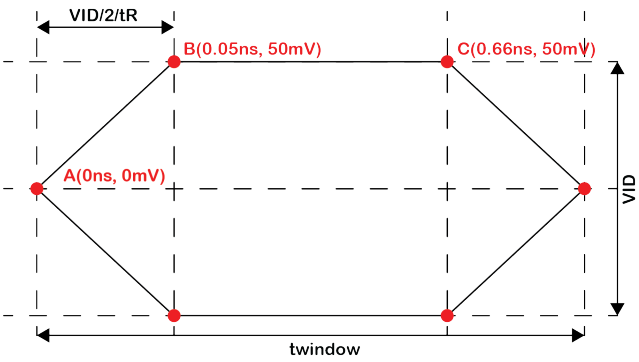


Figure 4: Eye Mask definition used to verify signal quality and timing in AEDT.

Results from this pre-layout analysis are displayed in Figure 5. As you can see, the eye is closed but does not violate the imposed mask. Taking into account that the lines is the 2D Transmission Lines Model were configured with a spacing of 250μm, this eye diagram is satisfactory enough.

2.5 Post-Layout Analysis - signal quality

After routing the Sub-LVDS lines and their associated reference planes from DLPC2020 to X3000 I exported the ECAD as ODB++ and imported it into Ansys Siwave where I performed a SYZ Sweep analysis with ports configured both for the IC and the connector, the result being exported as Touchstone file in Ansys Electronics Desktop. I removed the 2D

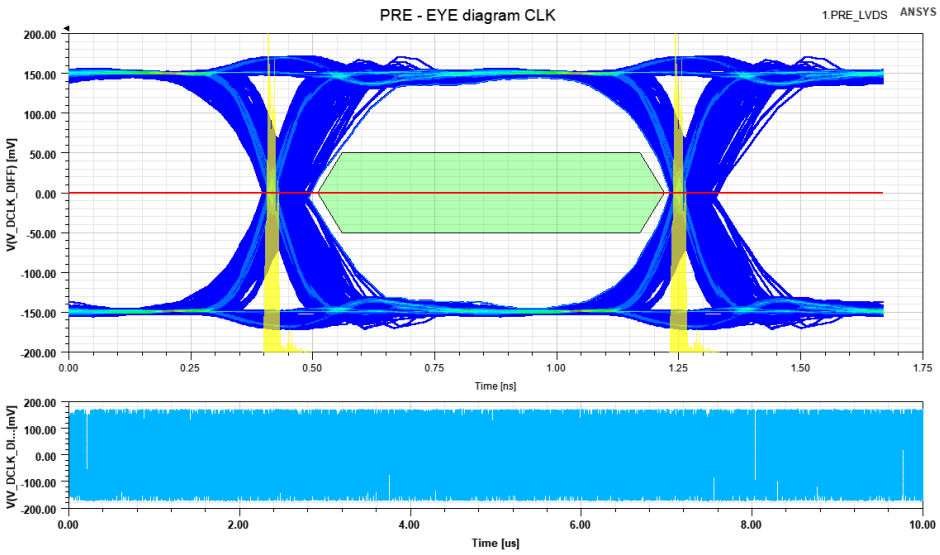


Figure 5: Pre-layout eye diagram for CLK signal.

Field Solver Transmission Lines Model and I inserted the extracted parasitic elements for the routed Sub-LVDS channel.

In this stage of the project I also included in the IBIS models of the CLK signal an additional Duty Cycle Distortion of 6% as stated in the datasheet of two ICs. Every post-layout simulation was performed with this distortion imposed on the actual signal to emulate a behavior as close as possible to the real expected one. The simulation file of this project, *TIEPLUS2020_DPSI_v1.aedt*, includes all of these simulation profiles. I also performed 5 post-layout simulations numbered from "2a" to "2e", one for every type of IBIS model (typical, fast, slow, min and max). The worst eye diagram was found for the slow model, also displayed here in Figure 6. However, the channel performances are still satisfactory.

Lastly, on the Signal Integrity topic I performed one more post-layout simulation with a variation from 80Ω to 120Ω with a step of 20Ω for the termination resistance of the differential pair. This resistor is internal to the DLP2020 IC and is therefore subjected to PVT variations. Since it was not included in the IBIS model, I opted to manually variate its values. The eye mask was still not violated under these circumstances.

3 Power Integrity

3.1 Pre-Layout Analysis - approximations

In this pre-layout stage a simple characterization of the power distribution network was made using analytical approximations. The VRM was described as a series RL circuit with the values provided in the description of the project. In the next paragraphs is described how each element of the PDN was modeled and approximated.

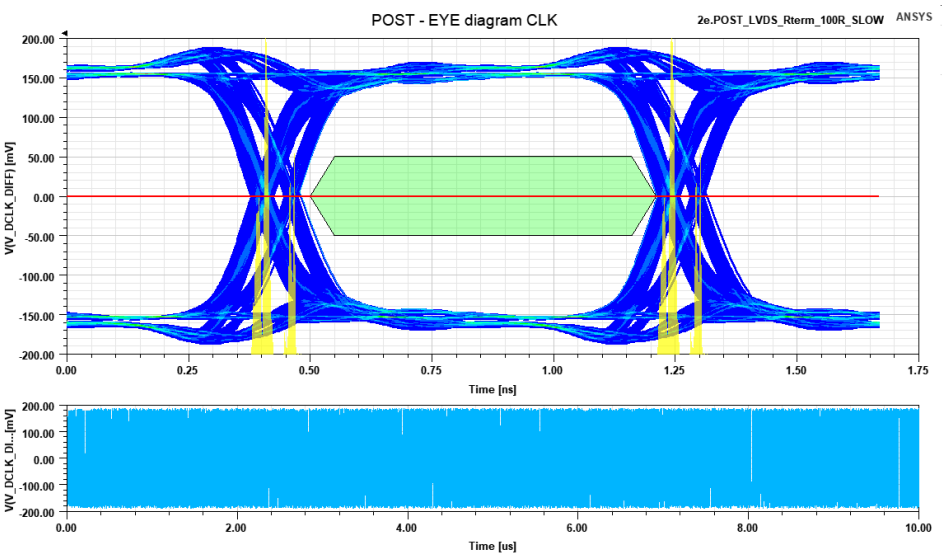


Figure 6: Post-layout eye diagram for CLK signal with IBIS model set to slow.

3.1.1 DCIR Resistance from VRM to DLPC2020

The DC resistance of a sheet of metal can be calculated using Equation 8 where t is the thickness of the metal foil and σ its electrical conductivity. However, due to skin depth effect, this value is only valid @DC since a higher frequencies the current tends to concentrate on the outer surface of the conductor. The effective thickness where the current is concentrated at a higher frequency can be calculated using Equation 10 and once is obtained an AC resistance can be calculated using Equation 9. However, this AC resistance is only valid at a specific frequency for which th skin depth was considered.

$$R_{DC} = \frac{1}{t \cdot \sigma} \cdot \frac{Len}{w} = R_{sqDC} \cdot n \tag{8}$$

$$R_{AC} = \frac{1}{\delta \cdot \sigma} \cdot \frac{Len}{w} = R_{sqAC} \cdot n \tag{9}$$

$$\delta = \frac{1}{\sqrt{f \cdot \pi \cdot \mu_0 \cdot \sigma}} \tag{10}$$

Another interesting aspect is the electrical conductivity of the planes involved in this investigation. For the GND plane buried inside the stack-up this constant is straightforward. However, for the VCC plane routed on the most outer layer of the stack-up, this is slightly different due to the plating of copper with Nickel and of the different electrical conductivity of these two metals. Using Equations 11 I obtained an equivalent electrical conductivity for the plated metal used for the VCC plane.

$$\begin{cases} \sigma_{Cu} = 5.8 \cdot 10^7 1/(\Omega \cdot m) \\ \sigma_{Ni} = 1.45 \cdot 10^7 1/(\Omega \cdot m) \\ \sigma_{Cu-Ni} = \dfrac{\sigma_{Cu} \cdot t_{Cu} + \sigma_{Ni} \cdot t_{Ni}}{t_{Cu} + t_{Ni}} = 3.27 \cdot 10^7 1/(\Omega \cdot m) \end{cases} \tag{11}$$

Using the numerical values from Equations 11 a DC resistance for the GND and VCC planes per square can be estimated using Equation 8. Alternatively, an AC @100MHz (considered an worst case scenario) resistance can also be obtained using Equations 9 and 10. Results from both the approaches are displayed in Equations 12 and 13.

$$\begin{cases} R_{sqGND(18\mu m)@DC} = 0.958 m\Omega \\ R_{sqVCC(43\mu m)@DC} = 0.727 m\Omega \end{cases} \tag{12}$$

$$\begin{cases} R_{sqGND(18\mu m)@100MHz} = 2.609 m\Omega \\ R_{sqVCC(43\mu m)@100MHz} = 3.510 m\Omega \end{cases} \tag{13}$$

Adding the results from Equations 12 and 13 I obtained the results from Equation 14. This addition is made since power and ground planes requires both of the planes for the current to spread and return from and to the VRM. How this resistance should be modeled is opened for discussion, since it has a DC value which increases with frequency. As a worst case value was desired, I included in my pre-layout simulation the worst case possible, **6.119mΩ** for the power planes structure resistance.

$$\begin{cases} R_{sqPLANES@DC} = 1.685 m\Omega \\ R_{sqPLANES@100MHz} = 6.119 m\Omega \end{cases} \tag{14}$$

3.1.2 Spreading Inductance from VRM to DLPC2020

Connecting the VRM to DLPC2020 through wide power planes will add a spreading inductance between these two components. This value can be estimated using Equation 15 where DLPC is inside a circle of radius a concentric to a larger one, of radius b on whose margin is residing the VRM. Based on the required placement drawing from slide 8/10 of the project description I estimated b to be around 43mm and a of 8mm (considering the power pins concentrated into the most inner 10 balls of the BGA).

$$L_{spread} = \frac{\mu_0}{2 \cdot \pi} \cdot h \cdot ln\left(\frac{b}{a}\right) \tag{15}$$

Equation 15 provides a result of **0.061nH** for the spreading inductance from VRM to DLPC2020. However, one should not trust this result too much since it is only accurate when the two concentric circles of radius a and b are placed far away from the margins of the planes, which is not the case in this design. When placed next to the margins, current crowding appears and spreading inductance might increase.

3.1.3 RC Series Characterization of Power Planes

The power planes will also add an additional capacitance to the PDN structure. This capacitance can be estimated using the parallel-plate approximation from Equation 16, where an average ε_r of 3.3 was considered. For a first order approximation, this averaged dielectric constant is good enough. In series with the parallel-plate capacitance there will also be an ESR (Equivalent Series Resistance) which can also be estimated using Equation 17 for a specific frequency. Once again, the 100MHz frequency was considered.

The value used for area in Equation 16 was roughly 2/3 of the total solid area where the VRM and DLPC2020 are situated. This consideration was made supposing that on the same layer of power the 1V8 rail should also be routed. The numerical results from these approximations are **Cpp = 102pF** and **ESR = 33mΩ**.

$$C_{pp} = \varepsilon_0 \cdot \varepsilon_r \frac{Area}{h} \tag{16}$$

$$ESR = \frac{Df}{2\pi f C_{pp}} \tag{17}$$

3.1.4 Spreading Inductance from Decoupling Capacitors to DLPC2020

Decoupling capacitors will be placed on the bottom side of the board to minimize as much as possible mounting inductance resulted from the parallel VIAs connecting the capacitor to the power planes. The BOTTOM side of the board will however be stitched with VIA stubs from fanouts since only a through-hole VIA is available, so capacitors will be placed on the perimeter of the BGA, where no other obstructions should appear. Equation 15 used with $h = 184\mu m$, $b = 15.1mm$ and $a = 8mm$ yelds a value of **0.023nH** for the spreading inductance from the decoupling capacitors to the DLPC2020 power pins. I should mention once again that the numerical value for a resulted from considering the power pins of IC3000 concentrated in the most inner 10 balls.

3.1.5 RL series Characterization of VIAs from DLPC2020 to power planes

The DLPC2020 IC will be connected through VIAs placed in a BGA quadrant style to the power planes situated near the opposite side of the board. This large height of 1.57mm of the loop will enlarge the loop inductance. However, this is not an issue since multiple pin pairs will be connected in parallel and this inductance will be reduced by the number of pairs. The same aspect applies to the series resistance of VIAs.

As far as the VIAs are regarded, the spacing between holes will be 0.8mm, the same size as the pitch between the BGA balls (power and GND pins are situated one next to the other). The outer diameter of the hole, D, is fixed at 0.2mm and the inner one, D', was considered to be 0.15mm. I considered this plating inside the whole to be the same thickness as the one of the board, of 25μm which is how the 0.15mm value for D' resulted. The number of power

and ground VIA pairs is fixed at 19, only the ones draining large current being considered. I ignored the ones from pins C3, H2 and J2 since these have very low values of current drained. All these parameters are synthesized in Equation 18.

$$\begin{cases} S = 0.8mm \\ D = 0.2mm \\ D' = 0.15mm \\ Len = 1.57mm \\ n = 19 \\ \sigma_{Ni} = 1.45 \cdot 10^7 1/(\Omega \cdot m) \end{cases} \tag{18}$$

Using Equation 19 I calculated the loop inductance per length for one VIA pair, L_{len}. The loop inductance of one pair was obtained by multiplying this with the length of the structure, Len. I obtained the total inductance, L_{total}, from all the VIA pairs by dividing this inductance with n, the number of VIA pairs. This total inductance was multiplied with a checkerboard factor of 0.8 which counts for the mutual coupling between VIA pairs that are not taken into consideration in this simple algorithm. Finally, this yelds a value of **0.057nH** for the total inductance in series with the IC.

$$L_{Len} = \frac{\mu_0}{\pi} \cdot ln\left(\left(\frac{S}{D}\right) + \sqrt{\left(\frac{S}{D}\right)^2 - 1}\right) \tag{19}$$

I used Equation 20 to calculate the resistance per length for each VIA pair, where D and D' values are the ones from Equations 18. The conductivity of the VIA was considered equal with the one of Nickel since this is the main plating material if ENIG is considered (Electroless Nickel Immersion Gold). I should mention that Equation 20 already has a 2 factor in its form which counts for both the signal and return VIAs. I obtained the resistance of one VIA pair by multiplying the result per length with the length of the structure, Len. Finally, the total resistance in series with the BGA chip was obtained by dividing the resistance of one pair with the number of pairs resulting in a value of **0.833m**Ω.

$$R_{len} = \frac{2}{\sigma \cdot (cross - sectionarea)} = \frac{2}{\sigma \cdot (\pi \cdot D^2/4 - \pi \cdot D'^2/4)} \tag{20}$$

In the above algorithm for the characterization of VIAs connecting the BGA to power and GND planes I ignored the skin depth effect due to the fact that effective area where the current travels is small enough to have this effect starting at larger frequencies.

3.1.6 Mounting Inductance for Decoupling Capacitors

Any mounting techniques used for the VIAs from the decoupling capacitor to the power planes will add some series inductance. However, if the loop formed by the two VIAs is as small as possible, this inductance is reduced. Placing the capacitors on the BOTTOM

side of the PCB contributes positively to this reduction since the loop height is diminished from 1.57mm (what would have been if capacitors where placed on the TOP side) to only 0.184mm. These values should be considered slightly smaller since the loop is from the capacitor body to the closest power plane, not to the farthest. However, a worst case situation was investigated here.

The body of the capacitor also has an important contribution to the mounting inductance. Lower case is always better, so the lowest possible one was used, 0402. By lowering the capacitor size, power and ground VIAs are brought closer apart and loop inductance decreases. Moreover, since VIA-in-pad was allowed for this design, VIAs from the pair can be even closer one from another. The center to center distance for a 0402 capacitor footprint is only 1.1mm.

Using Equation 19 where $S = 1.1mm$, $D = 0.2mm$ and $Len = 0.184\mu m$, a loop inductance of only **0.175nH** results for a power and ground VIA pair used to connect a 0402 decoupling capacitor to the power planes.

3.1.7 Mounting Inductance for Bulk Capacitors

Since the VRM has to be placed on the TOP layer and the power planes are buried near the BOTTOM part of the PCB, some VIAs will have to be added to cross the PDN network from the TOP to the BOTTOM part of the PCB. These VIAs are the same as the one mounting the bulk capacitors. In other words, I considered a good routing strategy to place the bulk capacitors near the VRM pins with almost no inductance in series (I ignored the small horizontal inductance) and further away from the VRM structure to penetrate the board with a pair of 4 VIAs which will add a vertical inductance calculated in exactly the same way as explained in Subsection 3.1.5, just that this time the spacing between VIAs will be larger, estimated roughly to 3.5mm (decoupling capacitors must have a 0603 case) and no checkerboard factor was further applied.

I estimated an inductance of 2.23nH per pair of VIAs and a loop resistance of 15.83mΩ (once again I ignored the skin depth effect for VIAs). Divided by 4, the number of VIA pairs near the decoupling capacitors, these numbers yeld a value of **0.557nH** for total inductance and **5.27mΩ** for total resistance. Importantly is to mention that these RL elements will be in series from the VRM to the DLPC2020 IC, since they are vertical structures which transition current from TOP to BOTTOM for the whole 1V1 power rail.

3.2 Pre-Layout Analysis - AC/DC PDN Noise Budget

With all the parasitic elements properly estimated as presented in the previous section, I now pass to the AC/DC PDN Noise Budget stage. From DLPC2020's datasheet, I extracted the minimum VDD voltage value as **1.045V** and the maximum as **1.155V**, values centered around the nominal **1.1V** value. These are the two limits of the voltage interval that should not be violated in any circumstance. Displayed in Figure 7 for further discussions is the

PDN Noise Budget Window. From the project description, slide 6/10 I extracted the VRM accuracy as $\pm 1.5\%$. This opens the budget analysis, with an interval from **1.0835V** to **1.1165V** reserved only for the VRM accuracy.

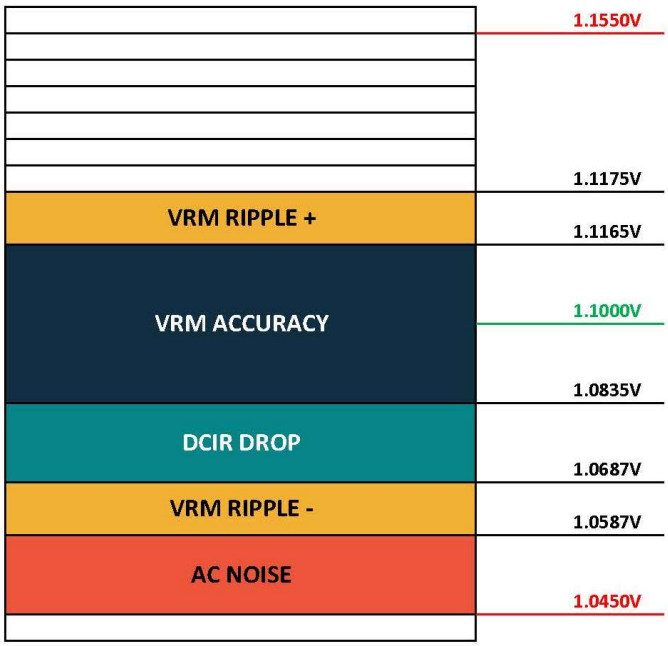


Figure 7: AC and DC PDN Noise Budget.

From the analytical approximations from the previous section, I can not calculate a total series resistance from the VRM to the DLPC2020 IC to estimate the DCIR drop voltage. This series resistance is composed of the internal VRM resistance, resistance of planes, of the 4 VIAs transitioning from Layer1 to Layer5 and 6 and of the 19 pairs of VIAs from the PDN to the BGA chip. This total resistance yelds a value of **37.22mΩ**. In Equation 21 the total voltage drop resulted from DCIR is calculated. Observe that a 0.2A was used for I_{leak} since the junction temperature of 88.44°C from Table 2 was considered. The DCIR drop lowers the voltage budget from **1.0835V** to **1.0687V**.

$$V_{DCIR} = (I_{leak} + I_{dyn}) \cdot R_{series} = 0.39A \cdot 37.22m\Omega = 0.0147V \tag{21}$$

From slide 6/10 I extracted the switching ripple of 10mVpp. Even if this ripple should be centered on an average value and the total addition to an existing voltage drop should only be of +5mV or of -5mV, I considered a full value of +10mVpp doubled of a -10mVpp in the PDN voltage to investigate the worst case possible. This resulted in a second interval from **1.0687V** to **1.0587V** with another identical one in the positive side of the budget.

The interval from **1.0587V** to **1.0450V** is what is left for the AC Noise. The $V_{ACnoise} = 1.0587V - 1.0450V = 0.01376V$ will define the impedance target for the frequency domain analysis as expressed in Equation 22. A Z_{target} of **70mΩ** was obtained by choosing the worst

case scenarios in each and every possible way. With this target defined, I move to pre-layout circuit analysis performed in Ansys Electronics Desktop with Nexxim simulator.

$$Z_{target} = \frac{V_{ACnoise}}{I_{dynamic}} = \frac{0.01376V}{0.196mA} = 70m\Omega \tag{22}$$

3.3 Pre-Layout Analysis - circuit simulations

3.3.1 Bulk Capacitor Optimization

With all the parasitic elements estimated and with an impedance target set I started a circuit analysis based on these values. These schematics and full simulation data is available for analysis in the directory *sim_AEDT*, project *TIEPLUS2020_PDN_v1.aedt*. Firstly, a 10μF capacitor for C26 was selected from Murata's online database, SimSurfing. A good candidate was GRM188Z71A106KA73. I tried as much as possible to select only X7R capacitors (an exception is C2002 which has a X7S temperature characteristic). Also about capacitors, each downloaded model was before biased at 1.1V (DC voltage of the investigated power line) and at a certain temperature.

I firstly optimized the PDN performances with capacitors biased only at the room temperature of 25°C and then I verified how the PDN behaves also at 89°C and at -40°C. If the lower -40°C was arbitrary chosen, the upper one resulted from Table 2 by assuming that the capacitors placed on the board have the same temperature as the board.

Displayed in Figure 8 is the impedance profile from the IC's perspective when only one 10μF bulk capacitor is included versus when this is multiplied with three. Multiplying it with three provides some additional damping to the resonant peak formed by this capacitors in parallel with the VRM structure. I decided to multiply the existing capacitor value and not to add another value to keep the different part list to a minimum. Adding more bulk capacitors would lower the peak below the target impedance but I decided to move to the decoupling capacitors since these too provide some damping to the parallel resonant peak.

Since the request of the project was to keep the impedance profile below the target up to the 20MHz frequency I could have added a few more bulk capacitors and the impedance would have dropped below the 70mΩ value at exactly 20MHz without any decoupling capacitor. This would be in my honest opinion a strange PDN ecology since a very large parallel peak would form between the on-die capacitance and package inductance in series with the board inductance if no decoupling capacitors were present.

3.3.2 Decoupling Capacitors Selection

I used the Frequency Domain Target Impedance Method (FDTIM) [2] for selecting decoupling capacitors values. Considering the 70mΩ target impedance and ESRs for 0402 capacitors as low as a few mΩ (for lower capacitance values such as 10nF which are not used in this investigation the ESR increases), a single capacitor from each value should be enough. Moreover, the value of 4700nF was omitted since its self-resonant frequency (SRF) was too

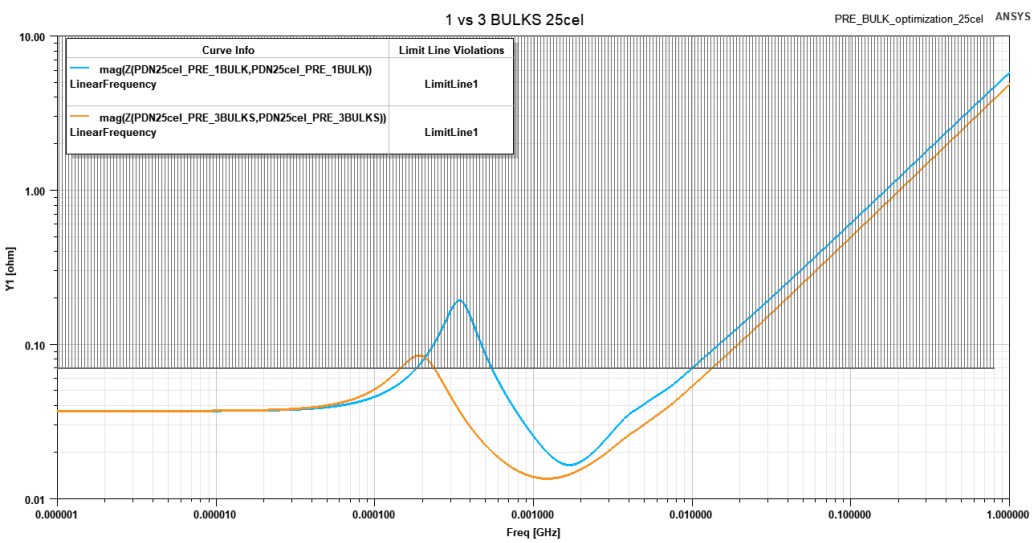


Figure 8: Impedance profile from the IC's perspective when only 1 bulk capacitor is included vs when 3 bulk capacitors are connected. t = 25°C.

close to the one of the bulk capacitors. Choosing only one capacitor from each discrete value available starting with 2200nF a stopped at 100nF because this one has a SRF of @20MHz when a 0.175nH mounting inductance is considered. Going any higher than this in frequency (lower in capacitance values) was not of interest since above this frequency in accordance with the project description the on-die capacitance should keep the impedance low.

Observe in Figure 9 the impedance profile from the IC's perspective for no decoupling capacitor and for the 5 distinct values capacitors placed. The inductance of the board after the last SRF point (of the 100nF capacitor) is greatly reduced since it is not composed roughly of the 5 total inductance of the decoupling capacitors. The capacitors used for decoupling with values ranging from 100nF to 2200nF are listed along with their manufacturer number in Table 3.

Table 3

Ref. Des.	Value	MURATA Part. No.
C26, C27, C28	10μF	GRM188Z71A106KA73
C2001	2200nF	GRM155Z71A225KE01
C2002	1000nF	GRT155C71A105KE13
C2003	470nF	GRT155R71A474KE01
C2004	220nF	GRT155R71A224KE01
C2005	100nF	GCH155R71A104KE01

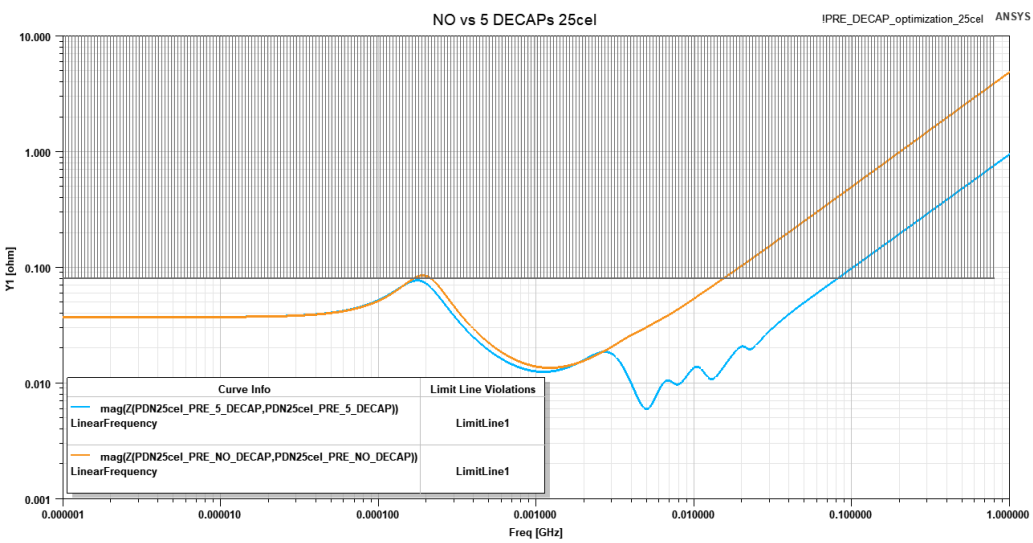


Figure 9: Impedance profile from the IC's perspective when only 3 bulk capacitors vs when also 5 decoupling capacitors are connected. t = 25°C.

3.3.3 Thermal Distribution Impact on Decoupling Capacitors

So far I have only performed the circuit simulations at room temperature, at 25°C, with capacitors biased at this specific value for temperature. Displayed in Figure 10 are three impedance profiles from the IC's perspective at the different temperatures of -40°C, 25°C and 89°C, the last one being of interest for this investigation since it is the temperature which capacitors will have once the system is powered up (if no thermal resistance is considered between the board and if they are considered fully passive).

Observe from Figure 10 how both the 25°C and the 89°C met the impedance target profile, with the rogue one being the -40°C one. From a PDN perspective, a higher temperature is better, at the extreme opposite corner being the -40°C profile probably because the ESR increases while temperature decreases.

3.4 Post-Layout Analysis - Ansys Siwave

I imported as ODB++ the completed ECAD in Ansys Siwave and I configured the required parameters (VIAs as plated with 25 μm of Nickel, conductivity of TOP and BOTTOM layer, dielectric constants, etc). All the Signal and Power Integrity simulations were performed using this tool.

For the DC analysis I configured in Siwave a voltage source with an internal resistance of 33mΩ, inductance of 33nH and a fixed voltage of 1.1V. Also, 19 current sinks were added, one at each power pin of DLPC2020. Each current source was referenced at the closest GND pin. The current drawn of each of these circuit elements was calculated by dividing the total 0.39A by 19 pins. After running a DCIR simulation I analyzed graphically the voltage results and a value of 1.088V at every IC ball was found. This corresponds to a total voltage

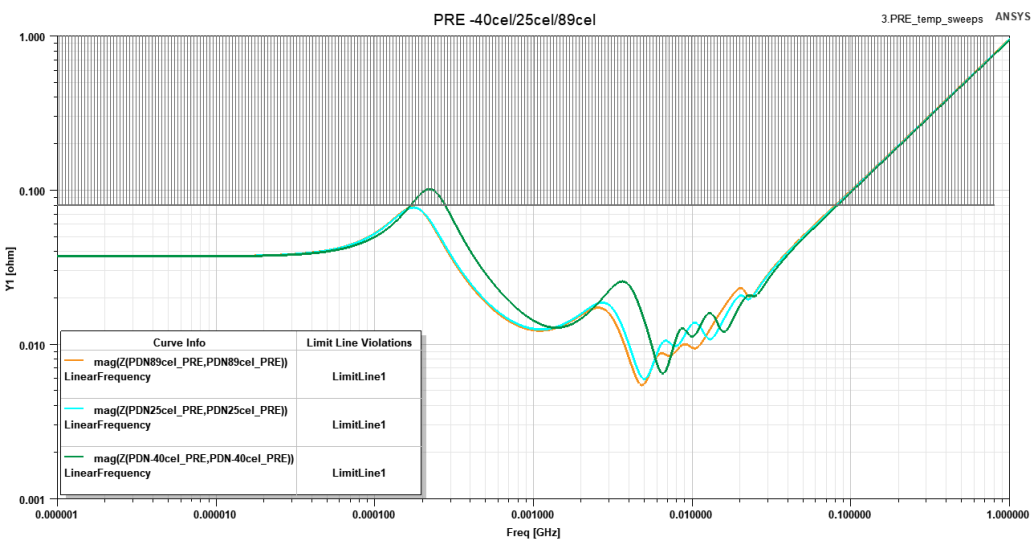


Figure 10: Impedance profile from the IC's perspective when 3 bulk and 5 decoupling capacitors are placed. Temperature curves for t = -40°C, 25°C and 89°C are included.

drop over the series resistance of 0.012V, very close to the initial estimate of 0.0147V from Equation 21.

Moving into the AC domain, I allocated from the internal Siwave capacitors database simulation models in accordance with values from Table 3 and I disabled the other ones of no interest for this simulation (I ignored completely capacitor C34 which decouples the VDDLP12). After setting individual ports for each BGA pin and for the VRM, I ran three different simulations, each with capacitors biased at the temperature of interest, and exported the Touchstone files in Ansys Electronics Desktop.

Plotted in Figure 11 are the three impedance profiles, one for each temperature, for the PDN resulted post-layout (exported from Siwave into AEDT). The same observations can be made as before, that strictly speaking, higher temperatures are better for this PDN structure. In the AEDT project of this investigation, *TIEPLUS2020_PDN_v1*, graphs comparing pre and post-layout analysis for different temperatures can be analyzed.

3.5 Post-Layout PDN Optimizations

After comparing the pre and post-layout impedance profile I concluded that I had to correct two numerical values from the initial assumptions: I decreased the mounting inductance of the decoupling capacitors from **0.175nH** to **0.050nH** (it was overestimated from the start) and I increased from **6.119mΩ** to **9.119mΩ** the resistance of planes. The two profiles have otherwise a good enough agreement at this point.

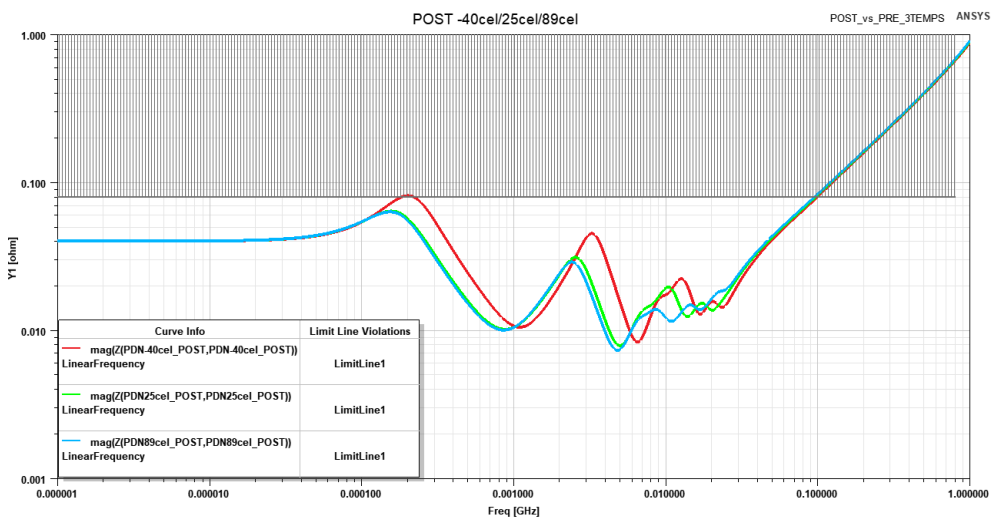


Figure 11: Impedance profile from the IC's perspective extracted post-layout using Ansys Siwave. Temperature curves for t = -40°C, 25°C and 89°C are included.

4 Conclusion

Further improvements can be made both in the ECAD design and in the simulation setup. In the ECAD part, the voltages +VBIAS, +VRST and VOFS were unfortunately placed too close to one differential pair of the Sub-LVDS channel. As far as the differential channel is regarded, there are isolated small islands near the X3000 connector where the return path is missing and maybe a better routing plan would have eliminated them.

As the Power Integrity filed is regarded, no analysis was performed on the 1V8 power line since it was outside the scope of this project. The 1V1 power line could be improved by using a better topology to penetrate from the TOP layer where the VRM is placed to the BOTTOM ones where the power planes are located. Very close power and ground VIAs would decrease the loop inductance associated with them and also multiple pairs would reduce the series resistance.

All in all, this project has been an interesting and also demanding task to fulfill, mixing fields of signal and power integrity now with thermal analysis. Using in this project directly on not a quarter of the subjects once learned in school and university gives me now a real insight into the high frequency and virtual prototyping fields. As far as my solution for the project and its correctness is regarded, I look forward to hearing what was done right and what was wrong.

References

[1] Eric Bogatin, *Signal and Power Integrity - SIMPLIFIED*. Prentice Hall, 2010.

[2] Larry D. Smith, Eric Bogatin, *Principles of Power Integrity for PDN Design - SIMPLIFIED*. Prentice Hall, 2017.

[3] S. C. Thierauf, *High-Speed Circuit Board Signal Integrity*. USA: Artech House, Inc., 2004. Propagation of Electric Fields in Exposed Microstrip. pp. 195–196.

[4] I. Novak and J. Miller, *Frequency-domain characterization of power distribution networks*. 01 2007.

[5] L. Simonovich and E. Bogatin, "Method of modeling differential vias." `http://lamsimenterprises.com/Method_of_Modeling_Differential_Vias-mod-Iss2.2-Apr2-12.pdf`. Accessed: 13 Oct 2020.