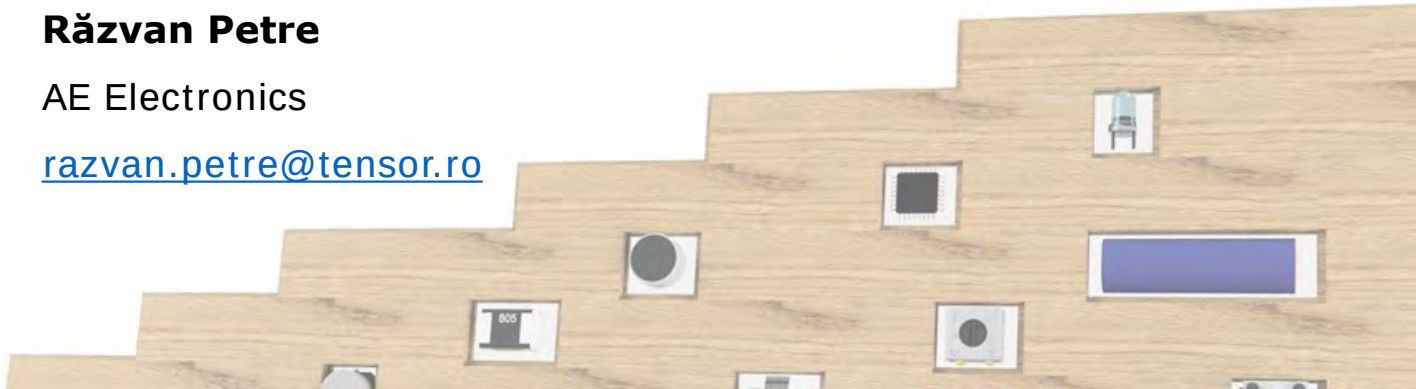
TIEplus 2020 challenge

Picture Generation Unit (PGU)

Răzvan Petre

AE Electronics

razvan.petre@tensor.ro



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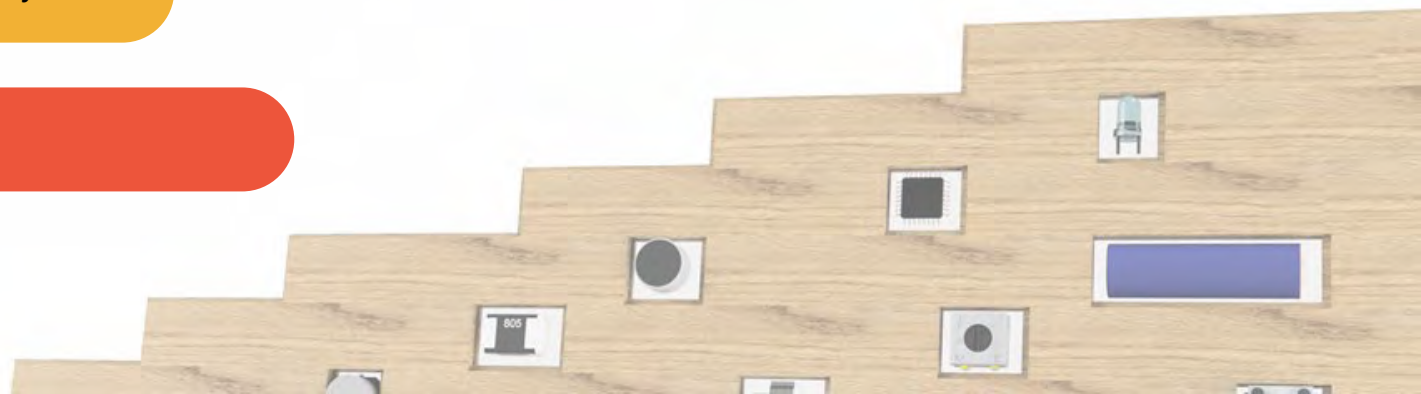

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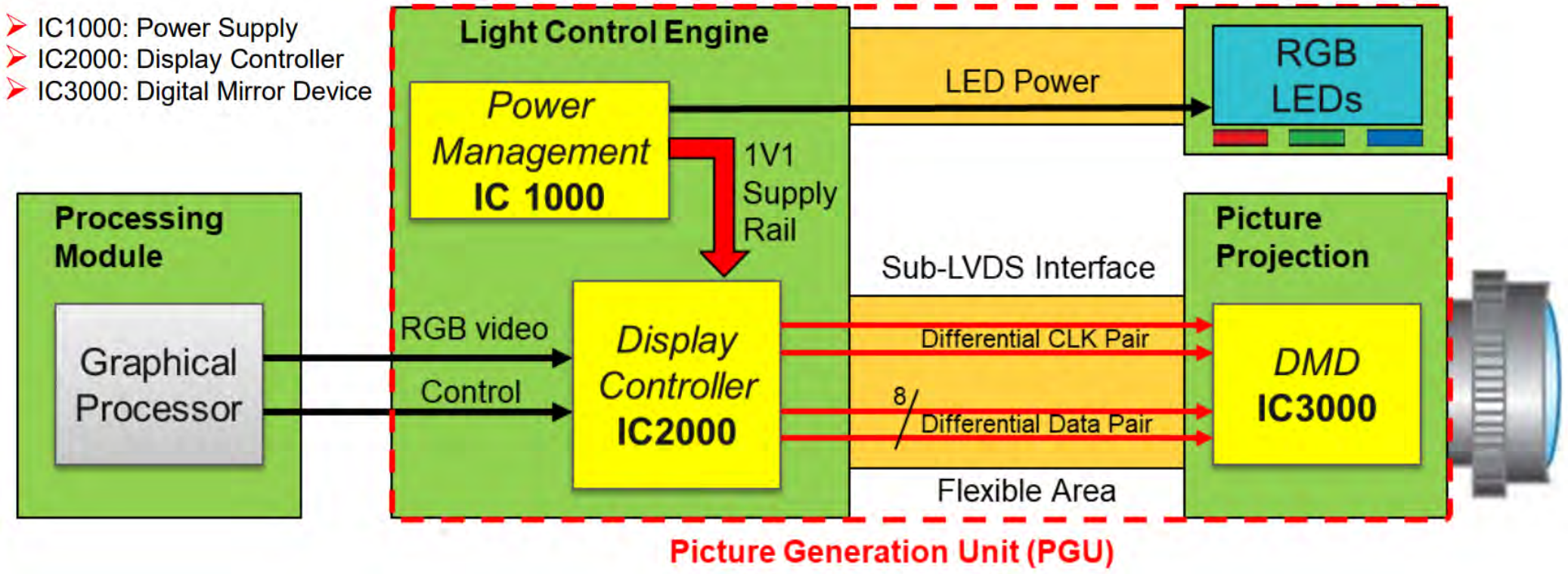
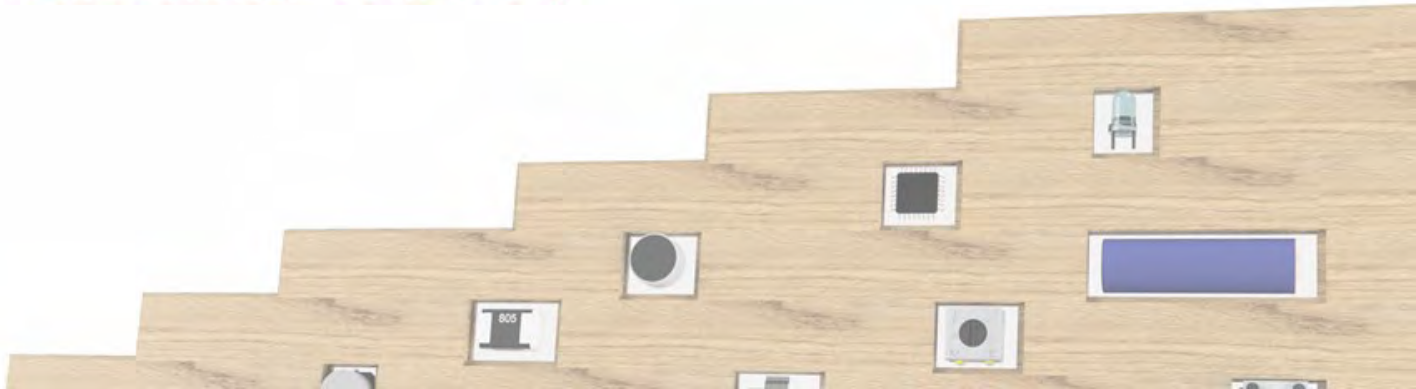


Figure 1 – Block Schematic



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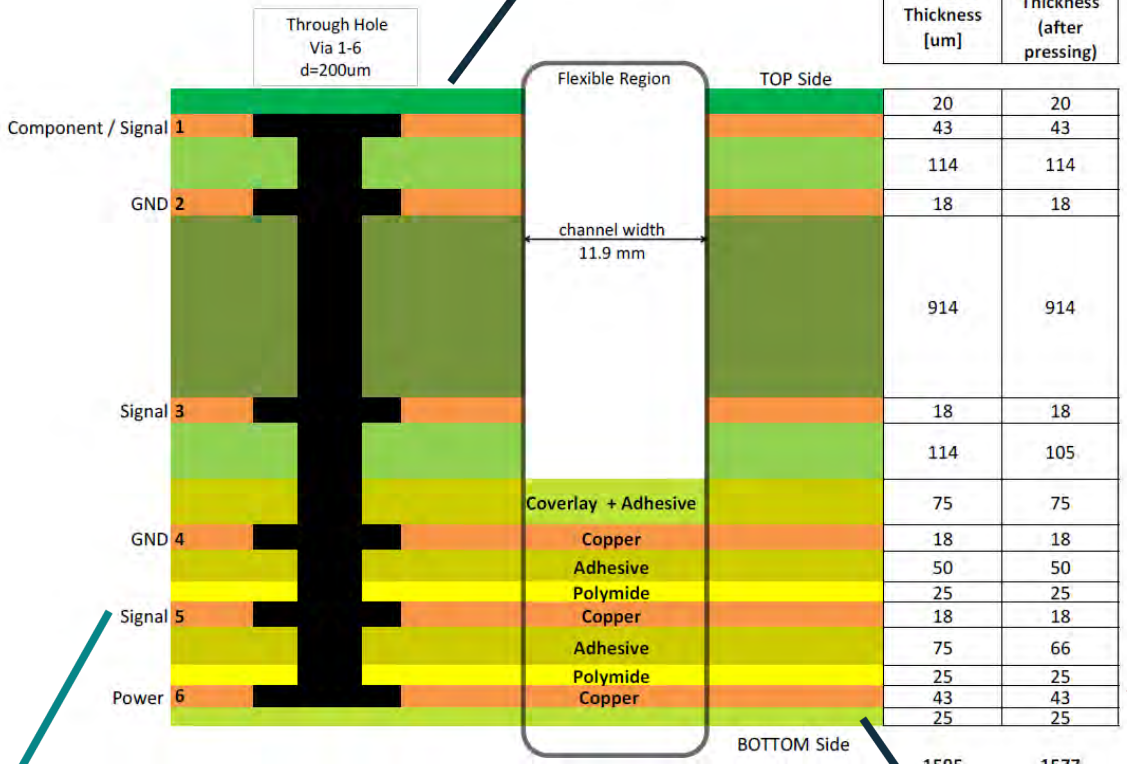


Nominal Thickness [um]	Final Thickness (after pressing)
20	20
43	43
114	114
18	18
914	914
18	18
114	105
75	75
18	18
50	50
25	25
18	18
75	66
25	25
43	43
25	25
1595	1577

IC1000
IC2000

GND plane

Power plane(s)

IC3000

Sub-LVDS

Figure 2 – PCB Stack-up

Equivalent Thermal Network

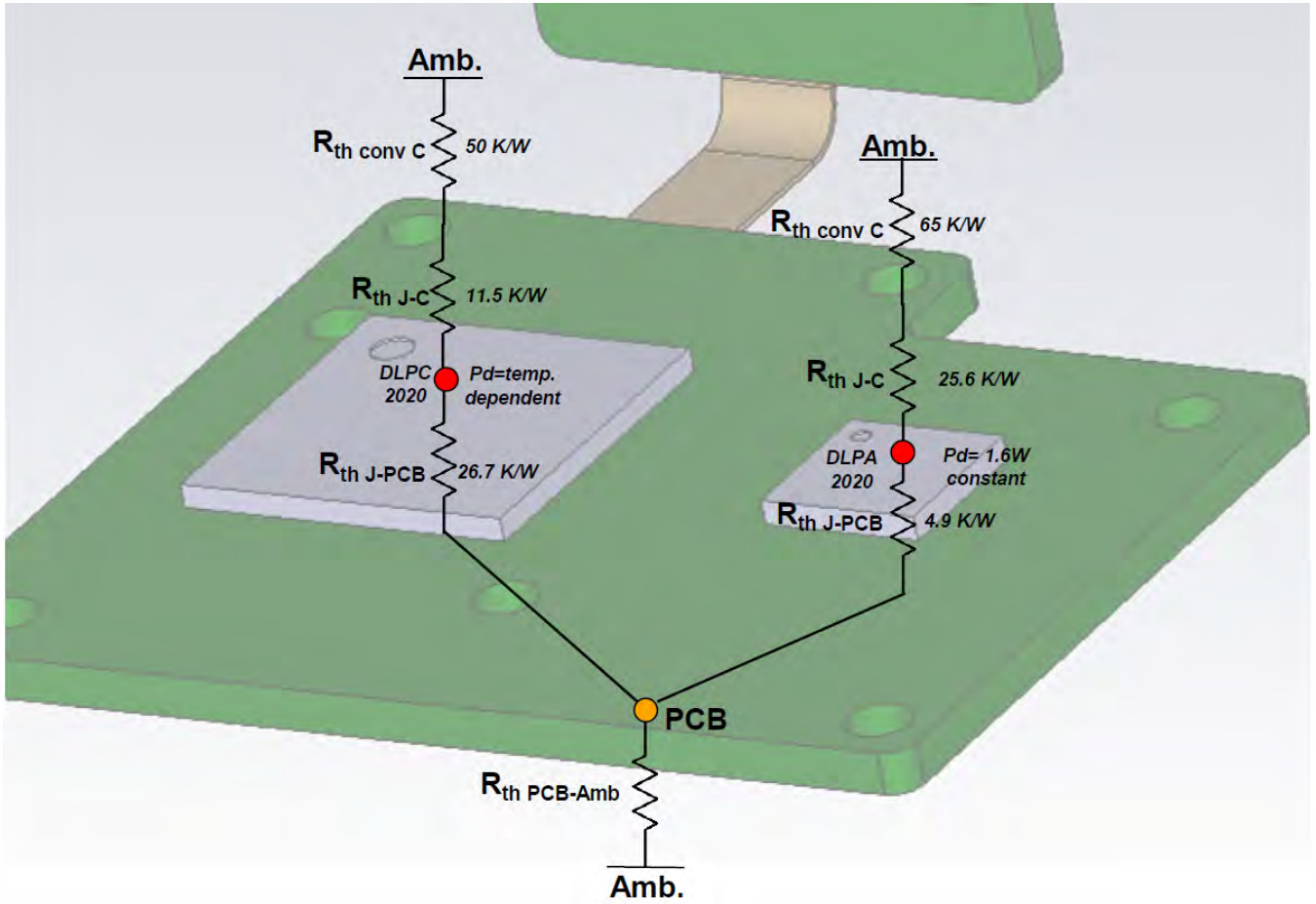


Figure 3 – Equivalent Thermal Network

Equivalent Thermal Network - preliminary

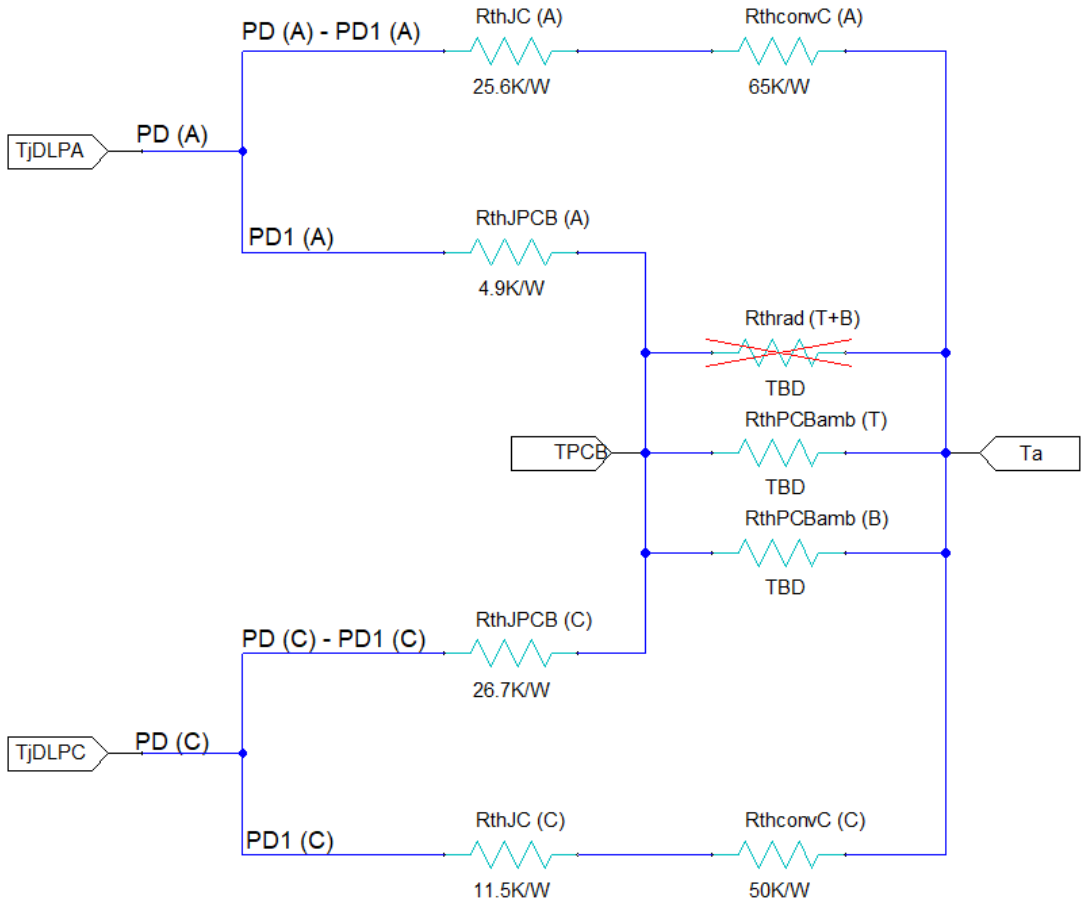


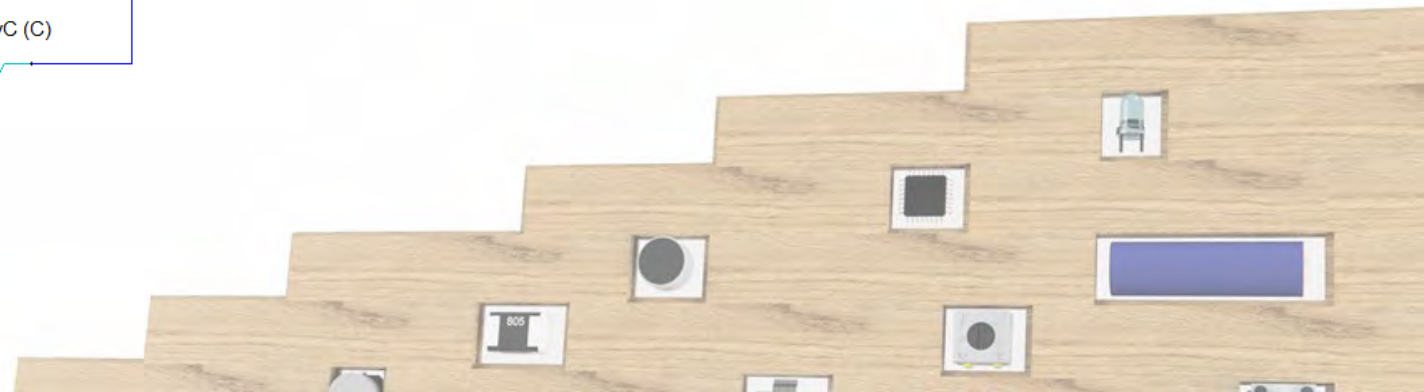
Figure 4 – Equivalent Thermal Network – preliminary

$$\begin{cases} R_{thPCBamb(T)} = \dfrac{1}{h_{TOP} \cdot A_{TOP}} \\ R_{thPCBamb(B)} = \dfrac{1}{h_{BOTTOM} \cdot A_{BOTTOM}} \end{cases}$$

Equation 1 – Thermal resistances of convection, TOP and BOTTOM

$$\begin{cases} h_{TOP} = 1.6 \cdot (T_{PCB} - T_a)^{\frac{1}{3}} \\ h_{BOTTOM} = 0.65 \cdot \left(\dfrac{T_{PCB} - T_a}{A_{BOTTOM}/P} \right)^{\frac{1}{4}} \end{cases}$$

Equation 2 – Convection Coefficients, TOP and BOTTOM



Thermal Analysis results - preliminary

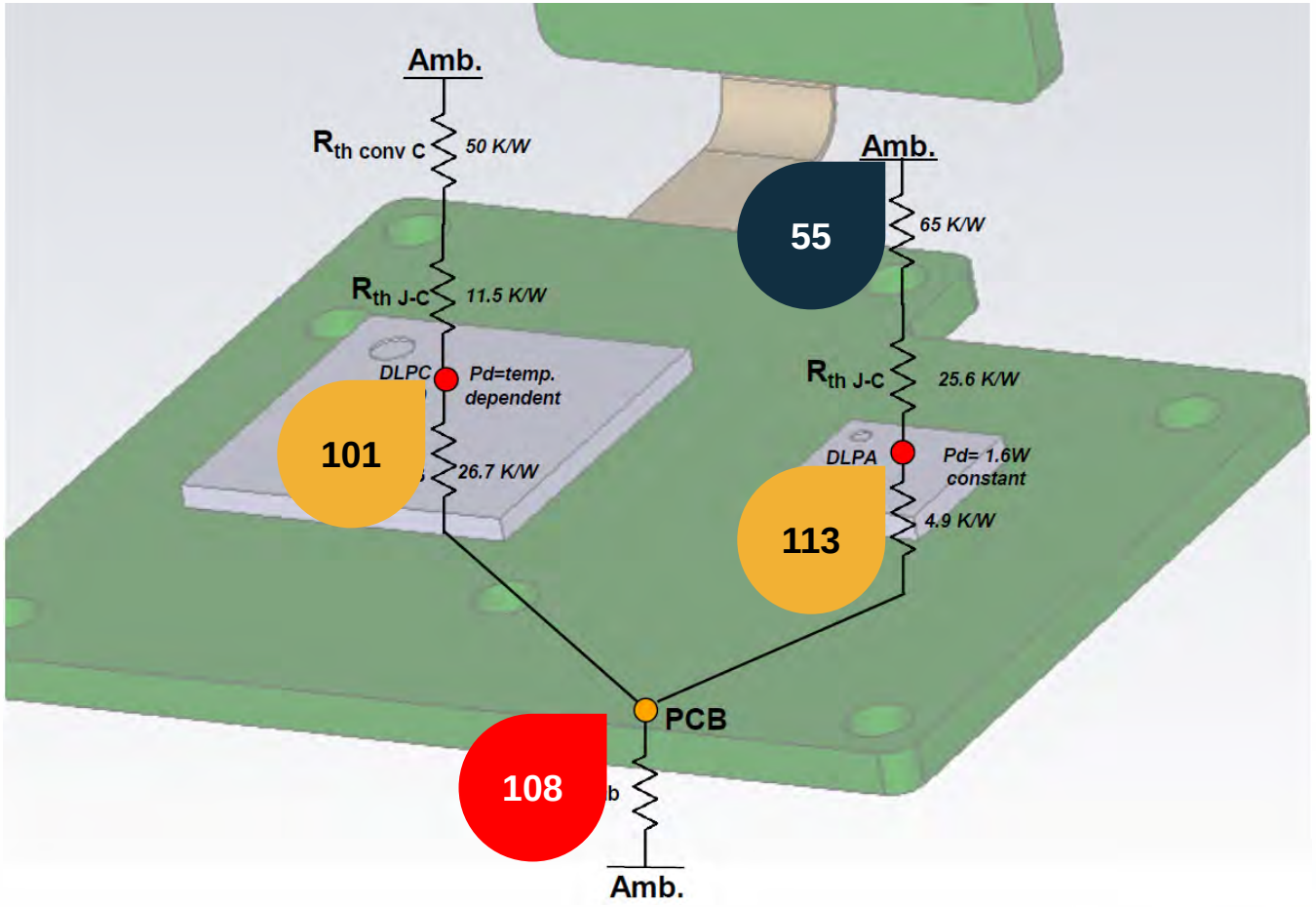


Figure 5 – Thermal Analysis results – preliminary. All temperatures in Celsius Degrees

Equivalent Thermal Network - improved

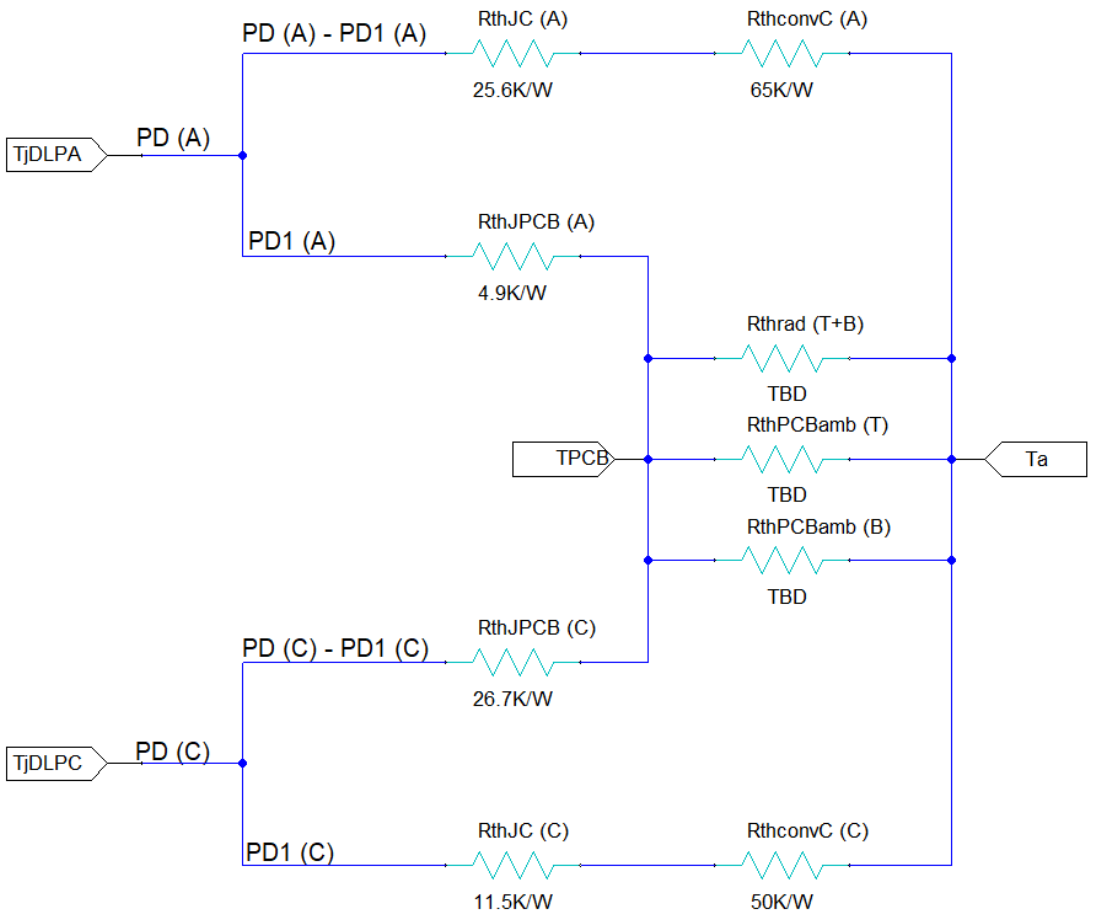


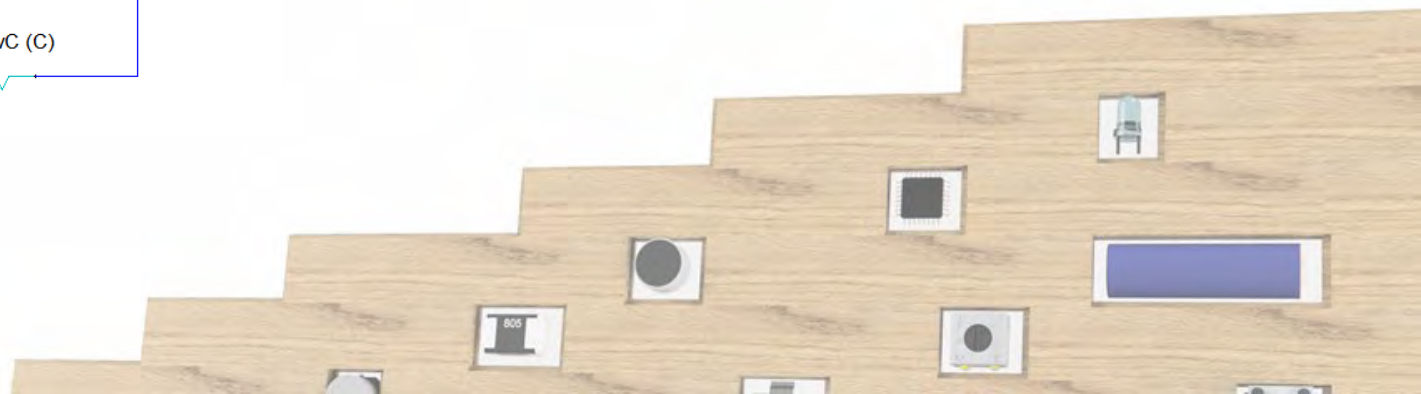
Figure 6 – Equivalent Thermal Network – improved

$$R_{thrad} = \frac{1}{\alpha_{radiation} \cdot (A_{TOP} + A_{BOTTOM})}$$

Equation 3 – Thermal resistances of radiation, TOP and BOTTOM

$$\alpha_{radiation} = \varepsilon \cdot \sigma \cdot (T_{PCB}{}^2 + T_a{}^2) \cdot (T_{PCB} + T_a)$$

Equation 4 – Coefficient of radiation, TOP and BOTTOM



Thermal Analysis results - improved

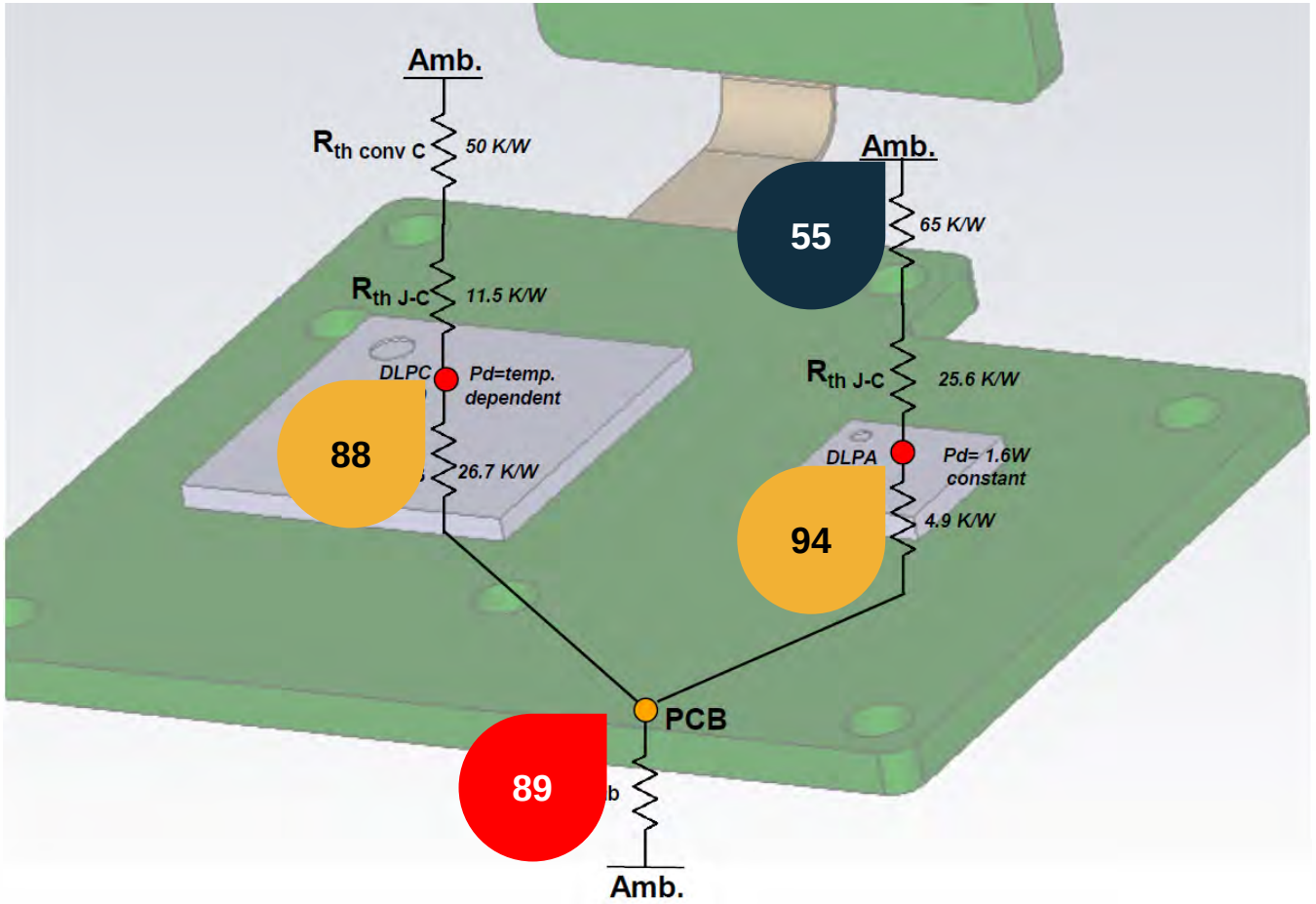


Figure 7 – Thermal Analysis results – improved. All temperatures in Celsius Degrees

Routing directives and strategy

- Signals routed on Layer 5
- Minimum number of VIAs: 2
- Zo = 50Ω, Zdiff = 100 Ω

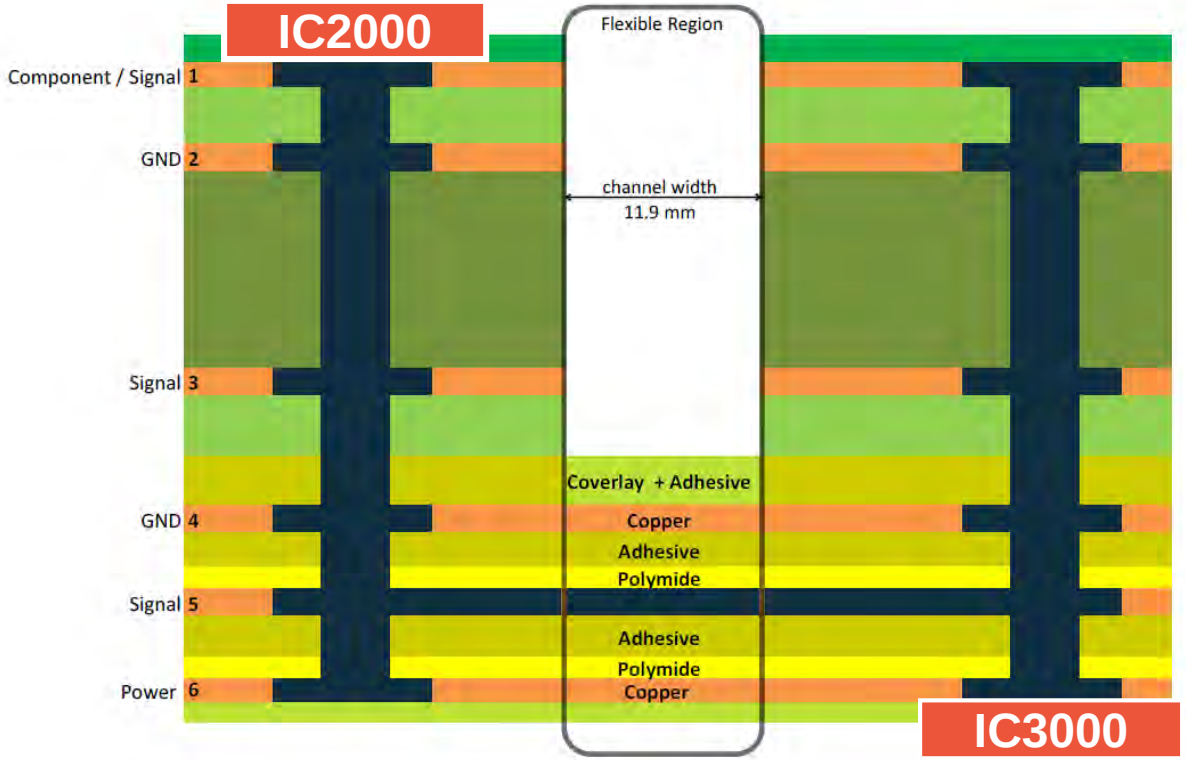


Figure 8 – Routing strategy for Sub-LVDS channel

Figure 9 – Trace width and spacing for Sub-LVDS channel routed exclusively on Layer 5

Differential VIA design pattern

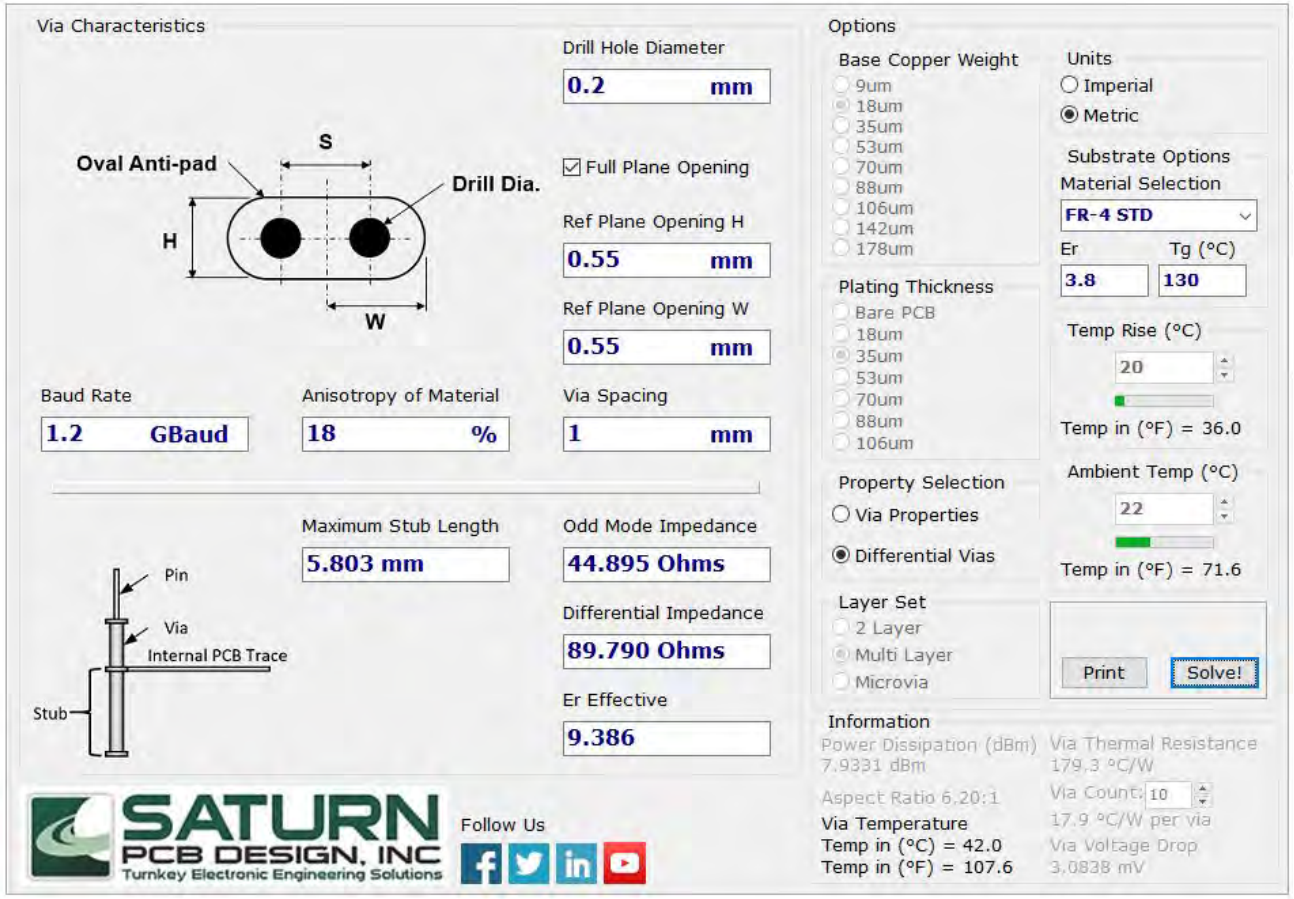
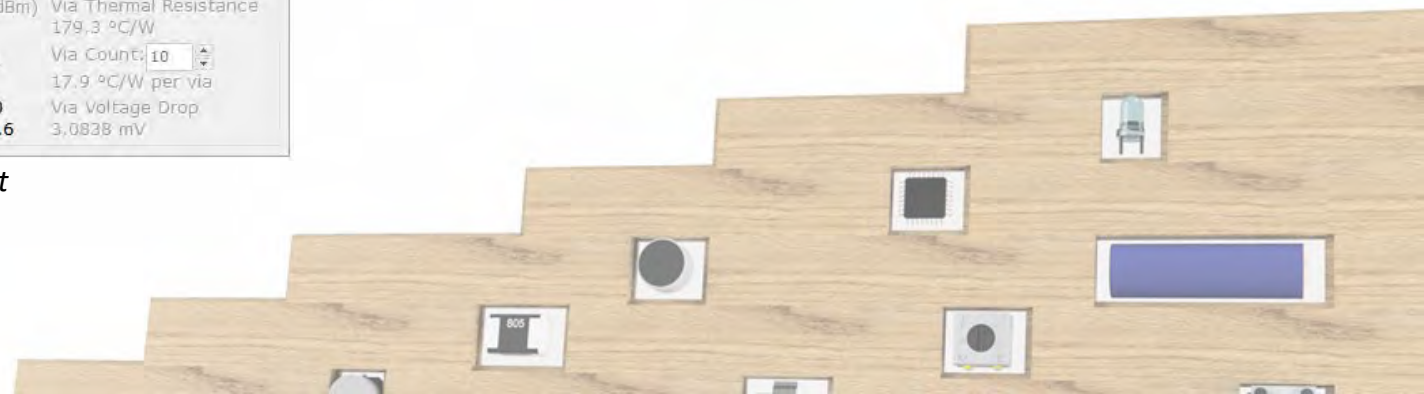


Figure 10 – Differential VIA design pattern – extract from SATURN PCB Toolkit

- "The Poor Man's PCB Via Modeling Methodology" by Bert Simonovich
- ZdiffVIA = 90 Ω



Intra-pair skew, in-pair skew, maximum etch length

Clock Switching Rate = 1200Mbps

Unit Interval (UINT) = 0.83ns

Window time = 0.71ns

Figure 11 – Timing constraints IC2000, IC3000

- Intra-pair skew = 10% * (0.83-0.71)ns = 0.012ns
- In-pair skew = 5% * (0.83-0.71)ns = 0.006ns
- Maximum etch length = 40% * 0.83ns = 0.332ns

Routing the Sub-LVDS lines

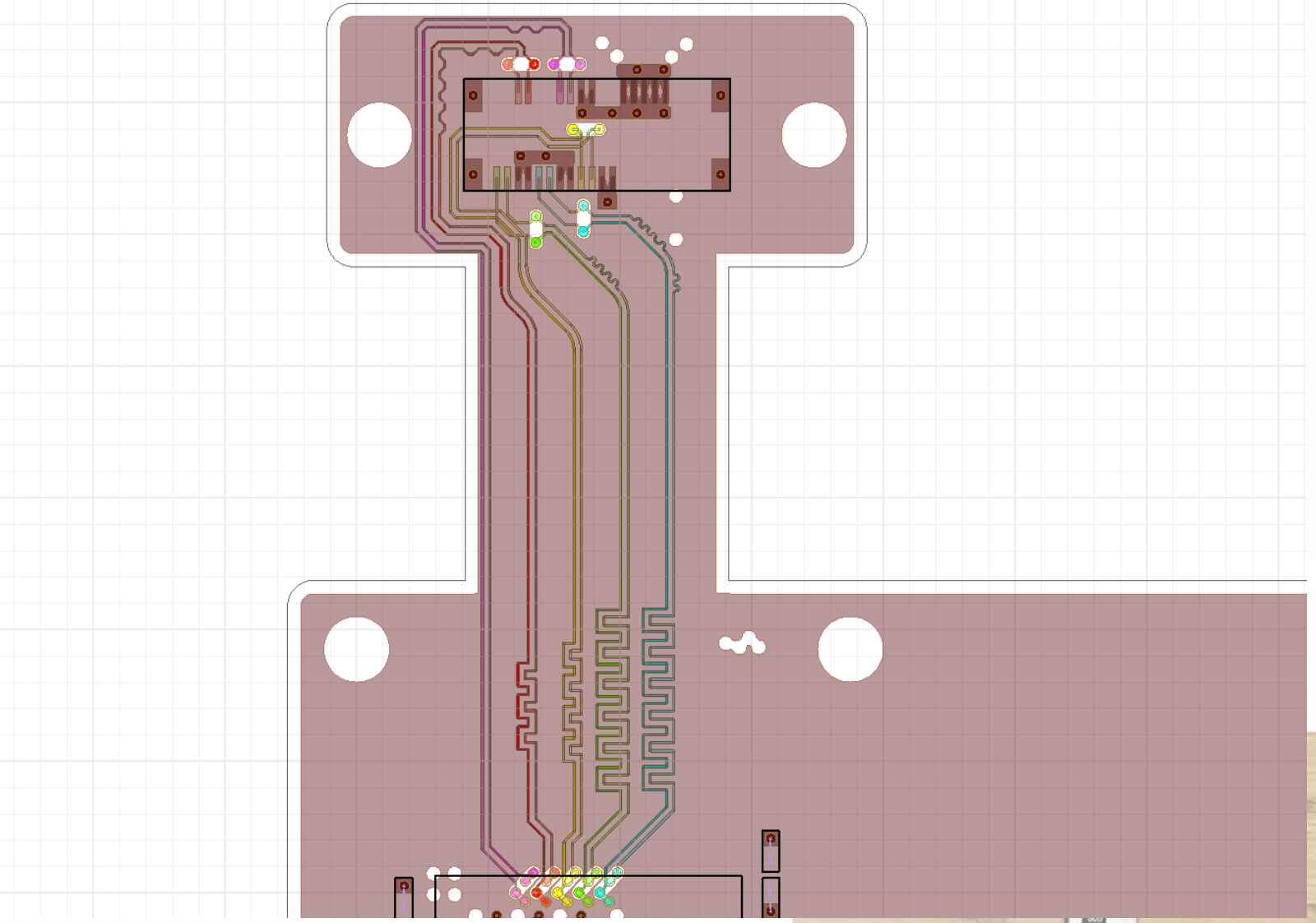


Figure 12 – Routed Sub-LVDS lines from IC2000 to IC3000

Evaluating Signal Quality – eye mask definition at IC3000

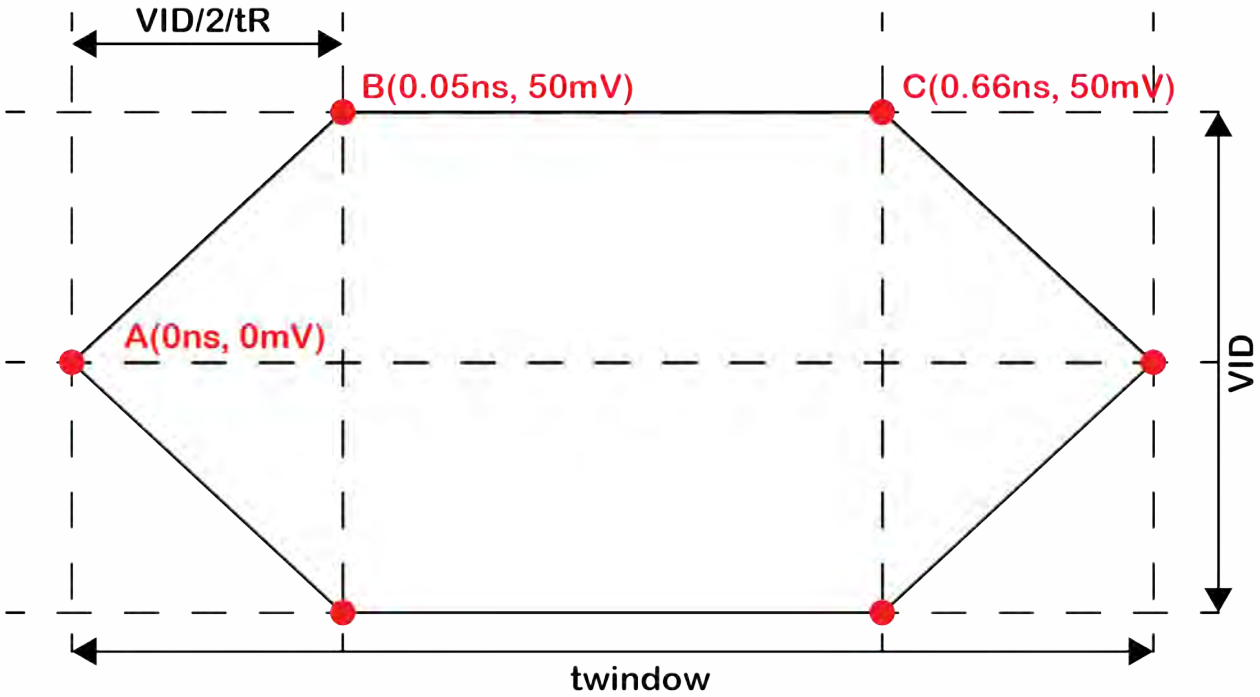
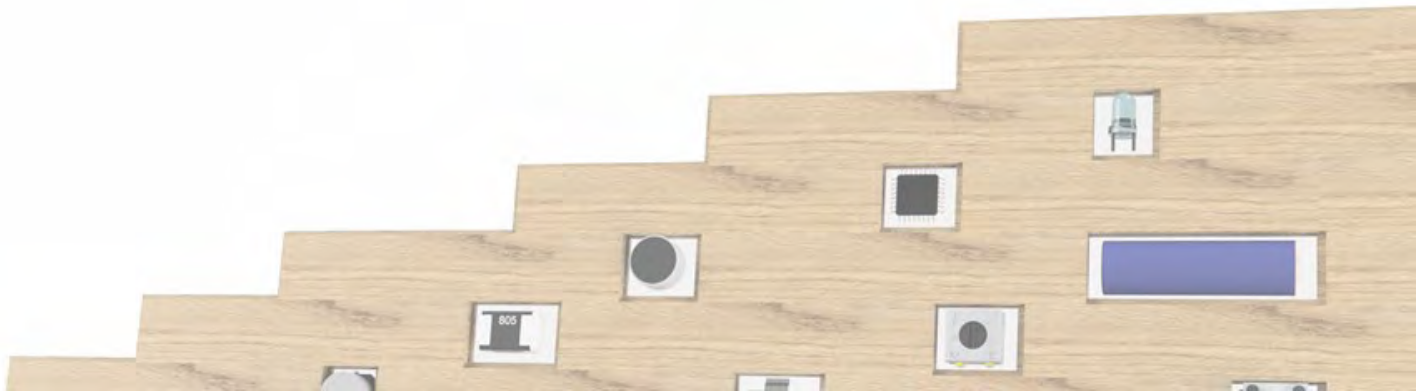


Figure 13 – Eye mask definition for DCLK, D0-D3

- Rise time = 1V/ns (worst case)
- Window time = 0.71ns
- Sub-LVDS differential voltage = **100mV**



Evaluating Signal Quality – ANSYS Electronics Desktop Setup

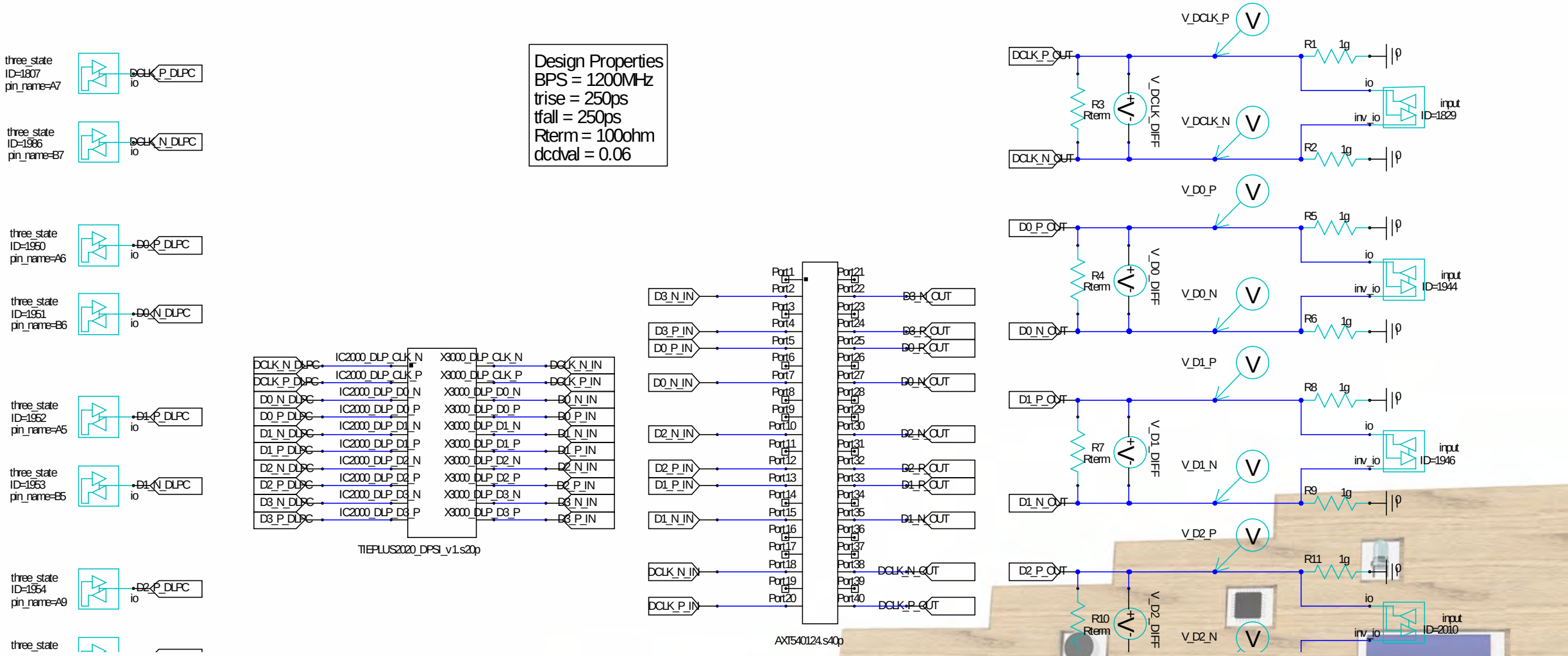


Figure 14 – ANSYS Electronics Desktop Setup, post-layout

Evaluating Signal Quality – Eye diagram(s)

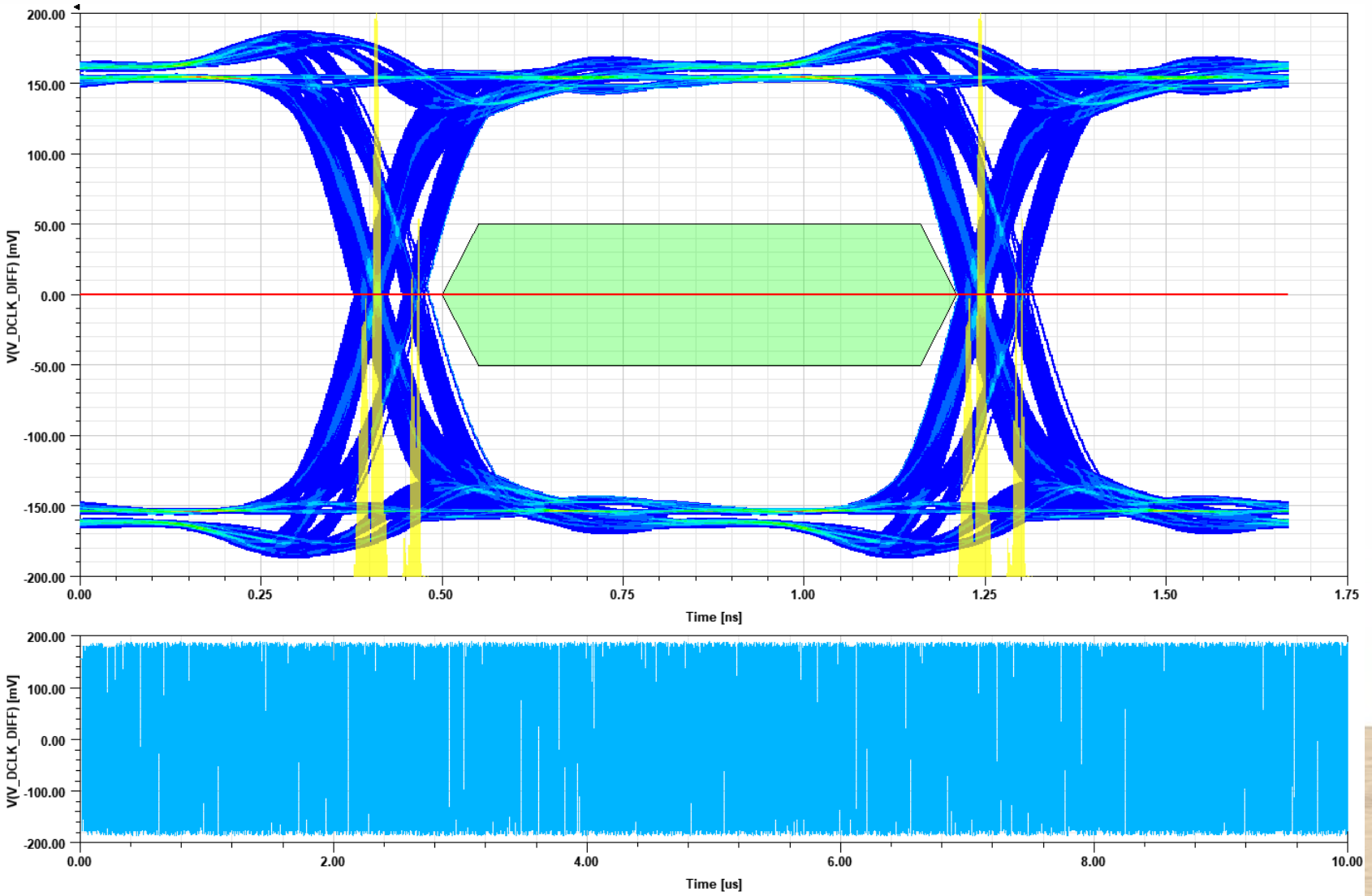


Figure 15 – Eye diagram for DCLK signal. 10us simulation time – 12048bits

- IBIS type = SLOW

Evaluating Signal Quality – Eye diagram(s)

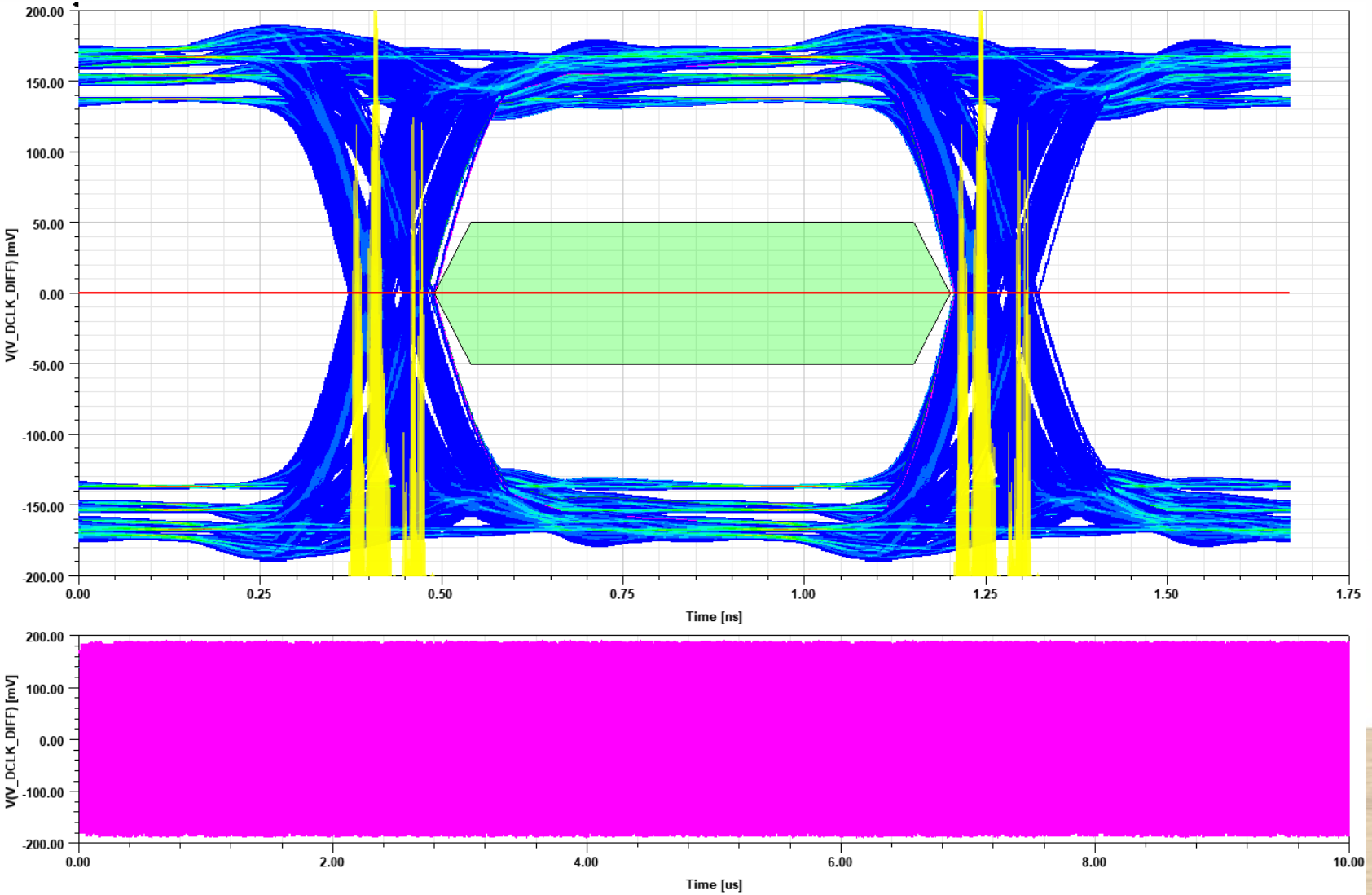
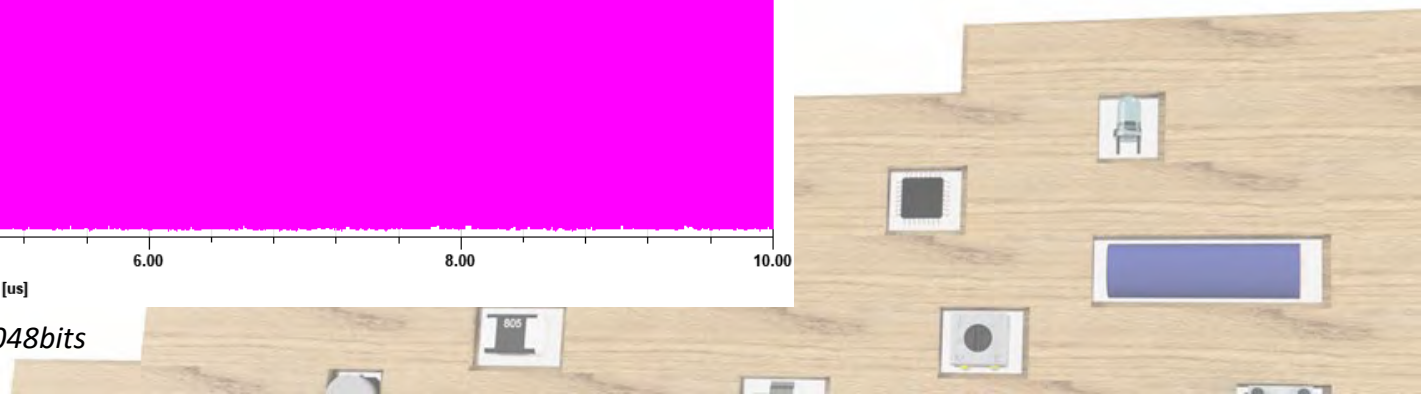


Figure 16 – Eye diagram for DCLK signal. 10us simulation time – 12048bits

- IBIS type = MIN
- Termination R swept from 80 to 120Ω



Pre-layout characterization of PDN elements

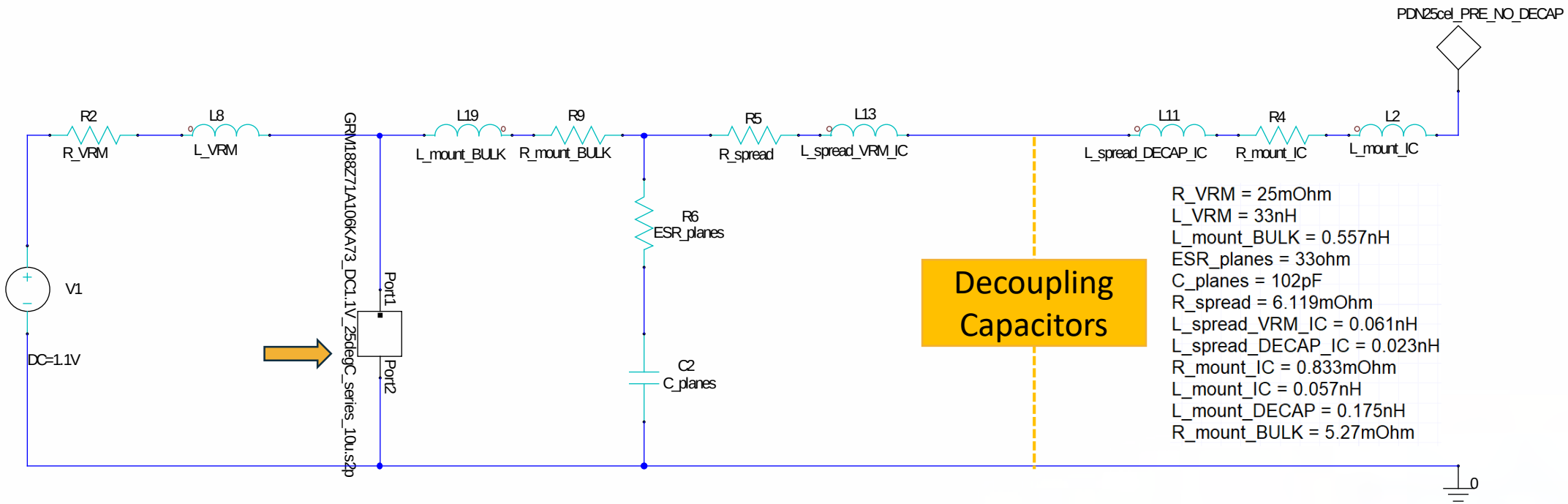


Figure 17 – Pre-layout characterization of PDN elements, only one 10uF bulk capacitor included. T capacitors = 25C.

- Total DC resistance = 25 + 5.27 + 6.12 + 0.83mΩ = **37.22mΩ**

AC and DC noise budget

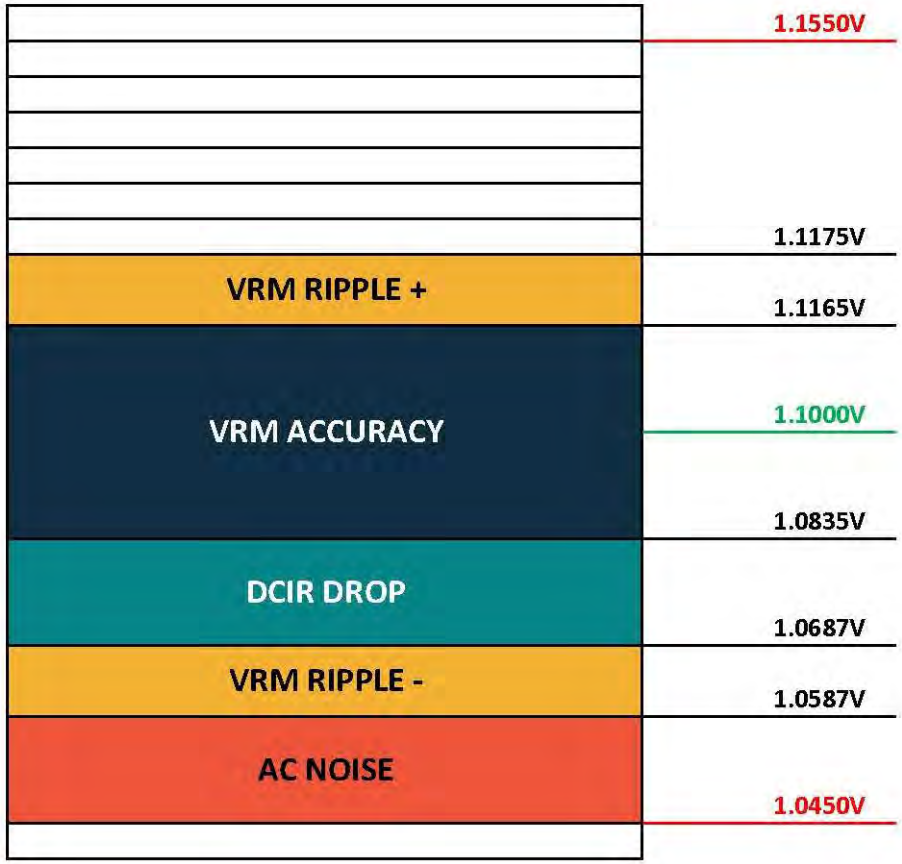
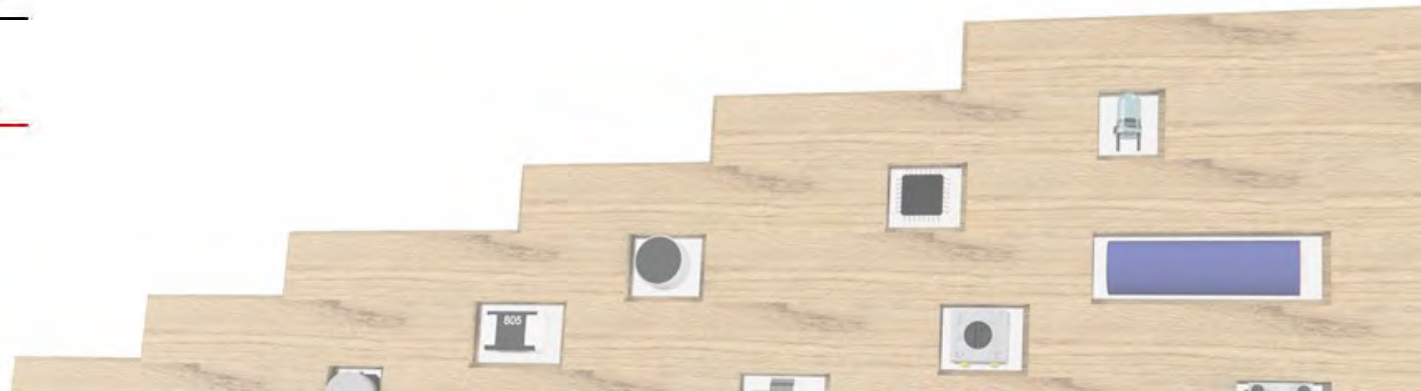


Figure 18 – AC and DC noise budget

- DCIR drop = (Ileak + Idyn) * DC resistance =0.39A * 37.22mΩ = **0.0147V**
- Z target = 0.01376V/0.196A = **70mΩ**



Impedance profile from the IC's perspective

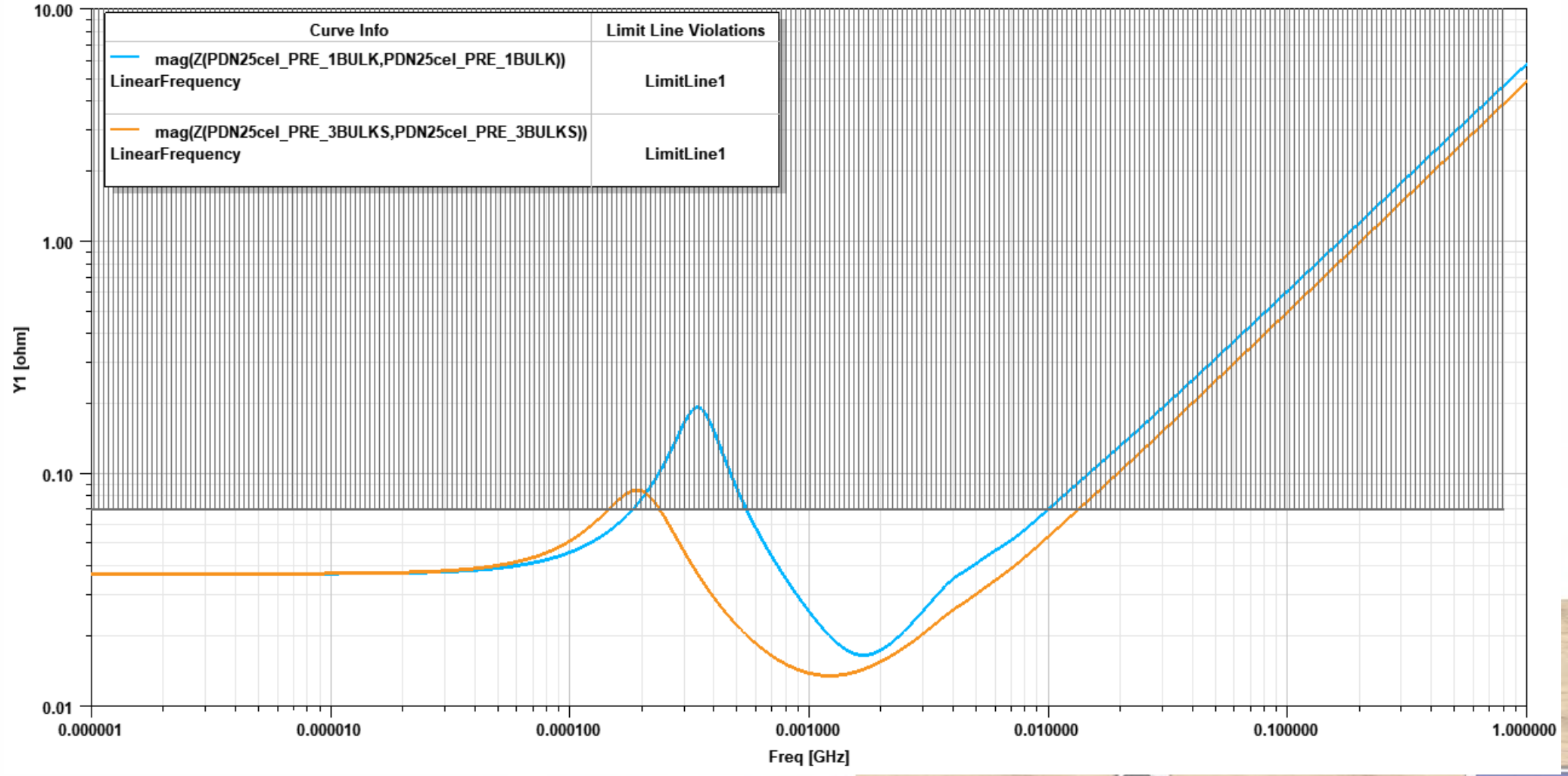


Figure 19 – Impedance profile from the IC's perspective.
1 vs 3 bulk capacitors, no decoupling. T capacitors = 25C.

Pre-layout characterization of PDN elements

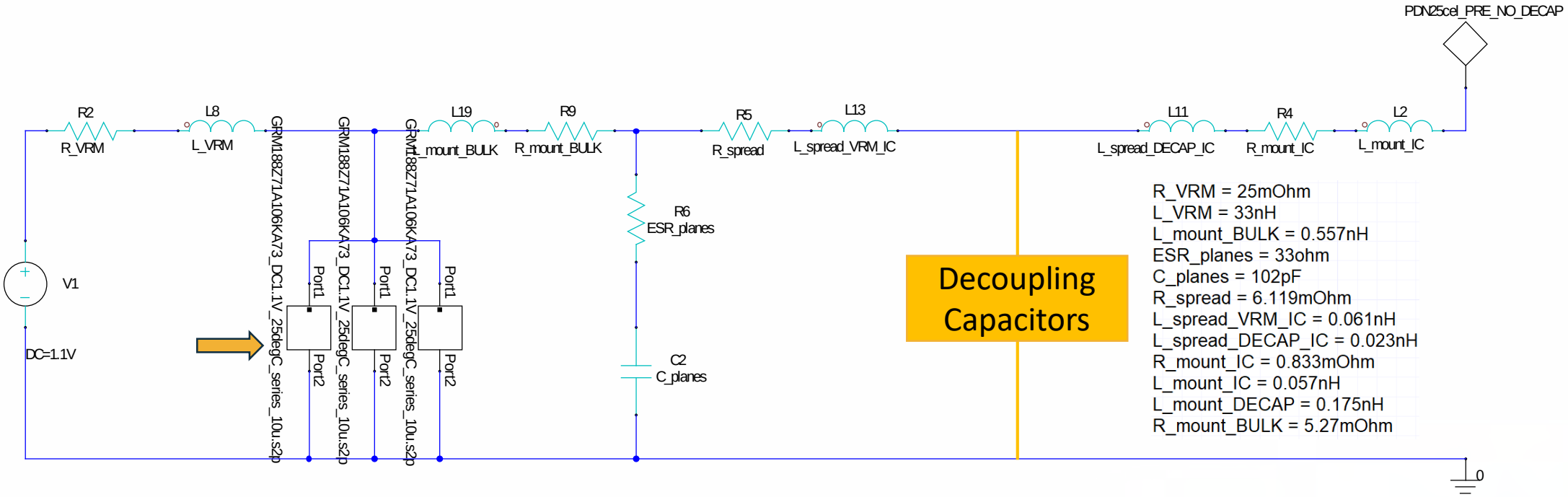
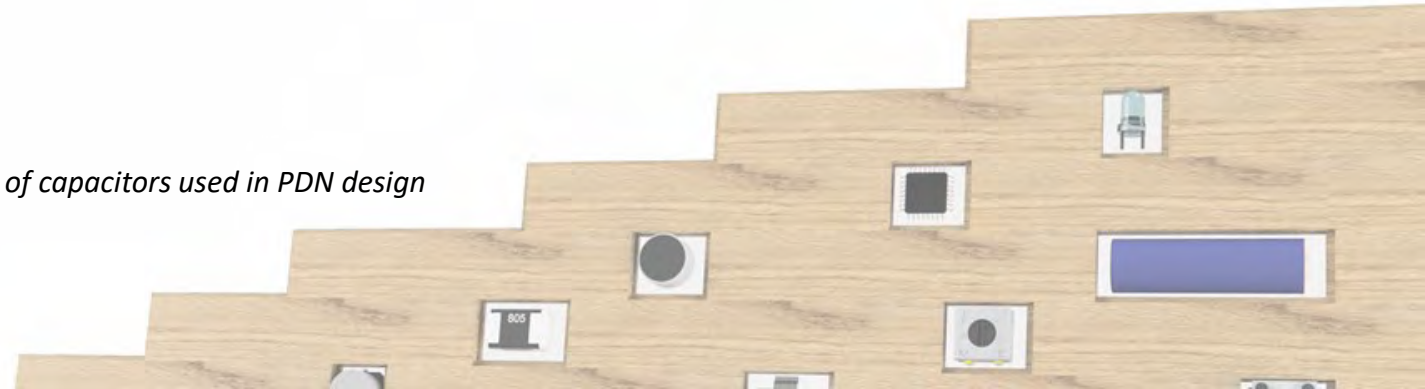


Figure 20 – Pre-layout characterization of PDN elements, three 10uF bulk and 5 decoupling capacitors included. T capacitors = 25C.

Ref. Des.	Value	MURATA Part. No.
C26, C27, C28	10μF	GRM188Z71A106KA73
C2001	2200nF	GRM155Z71A225KE01
C2002	1000nF	GRT155C71A105KE13
C2003	470nF	GRT155R71A474KE01
C2004	220nF	GRT155R71A224KE01
C2005	100nF	GCH155R71A104KE01

Table 1 – List of capacitors used in PDN design



Impedance profile from the IC's perspective

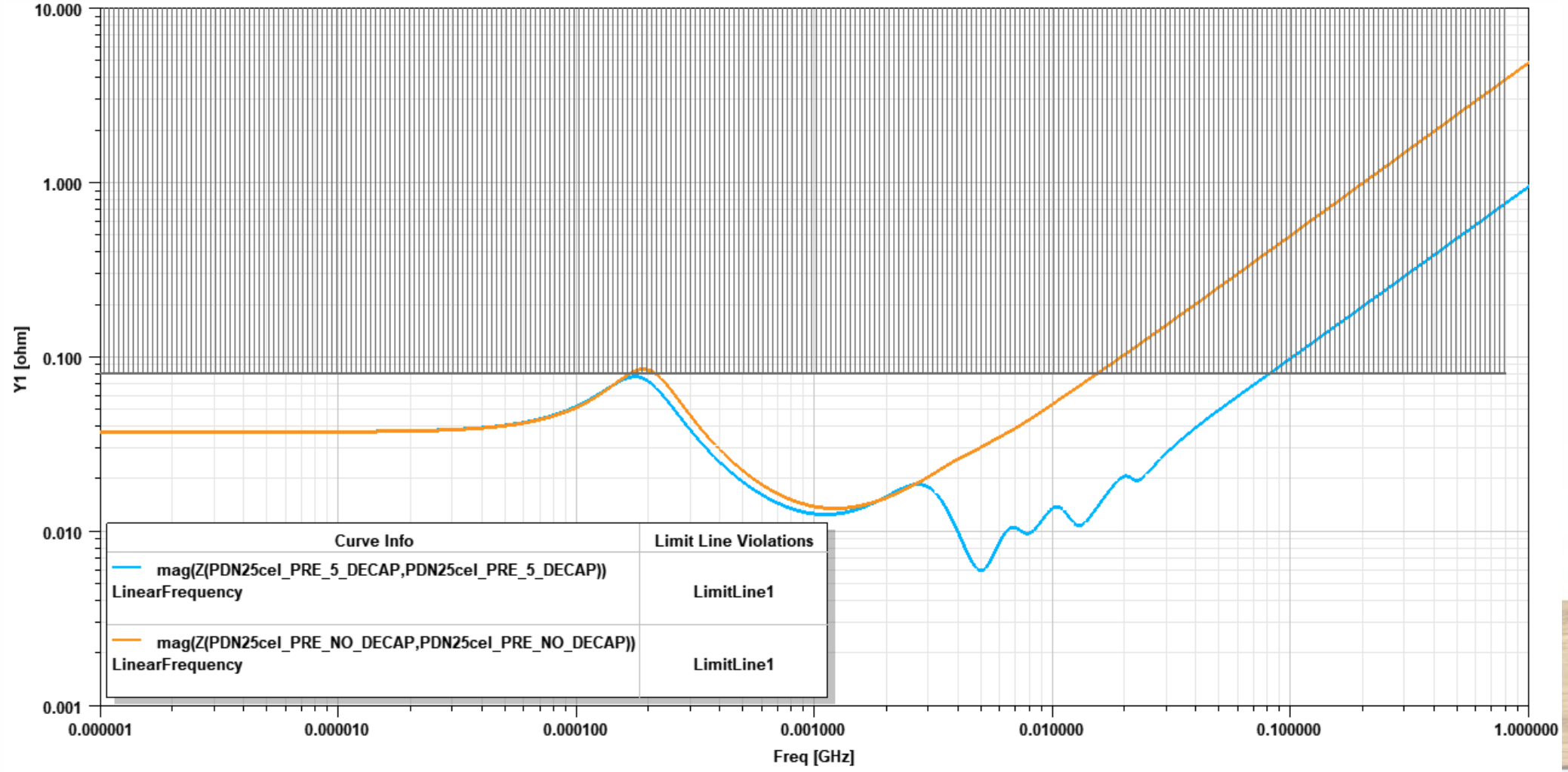


Figure 21 – Impedance profile from the IC's perspective.
3 bulk and 5 decoupling capacitors vs only 3 bulk. T capacitors = 25C.

Impedance profile from the IC's perspective

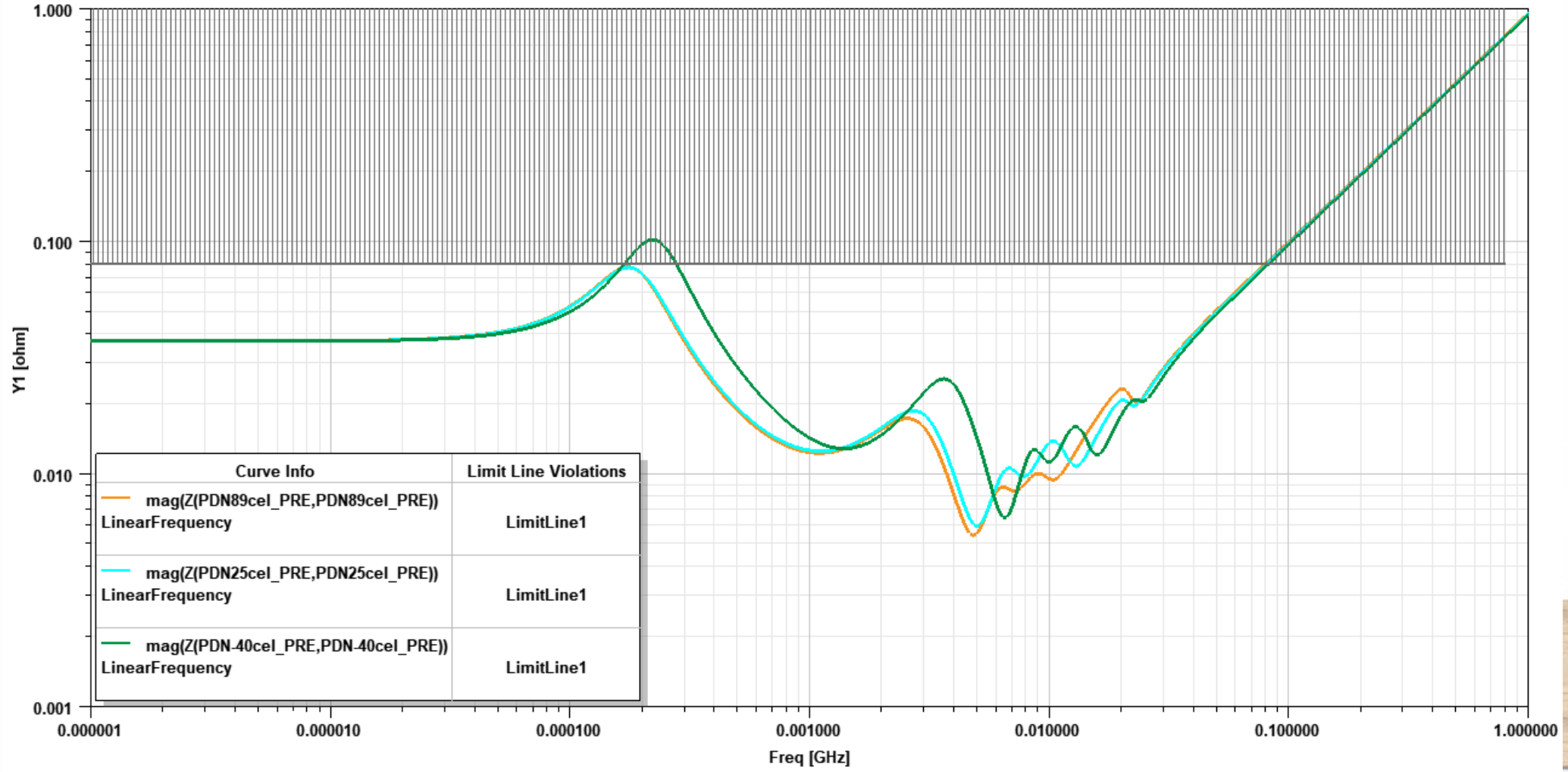


Figure 22 – Impedance profile from the IC's perspective.
3 bulk and 5 decoupling capacitors. T capacitors = -40C, 25C, ***89C.***

Post-layout parasitic extraction of PDN elements

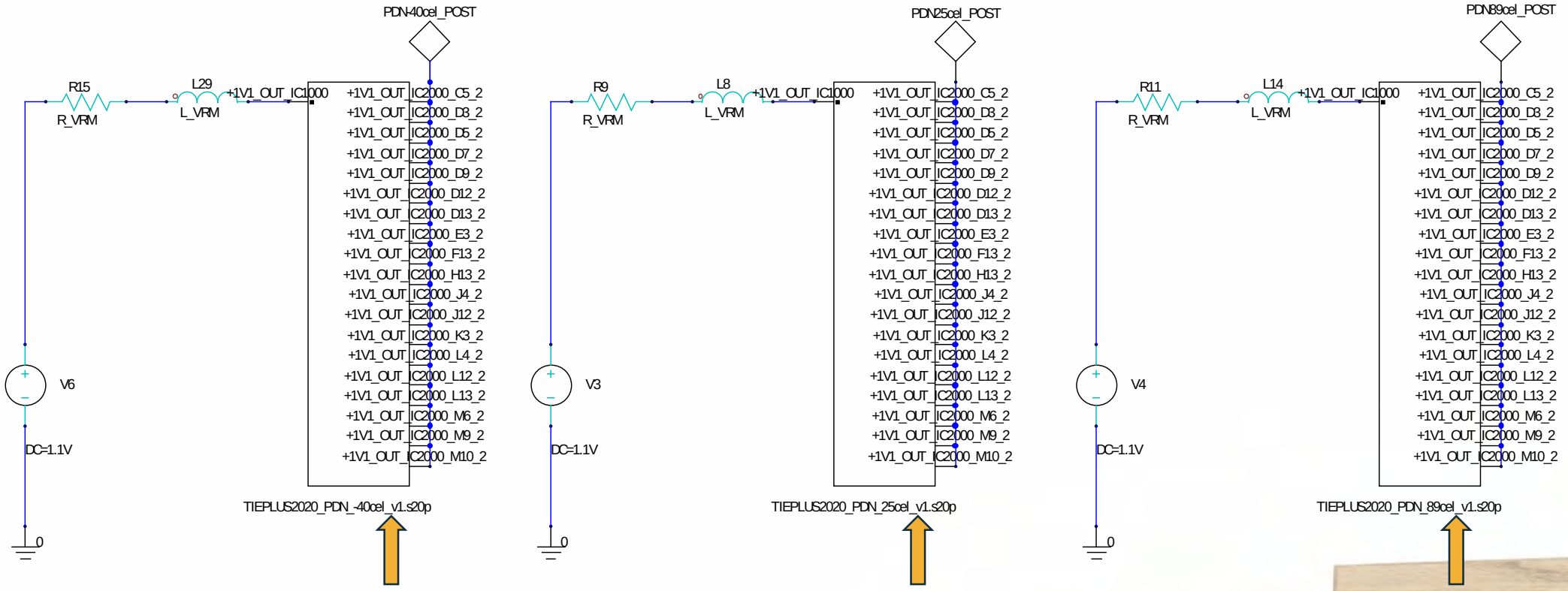


*Figure 23 – Post-layout parasitic extraction of PDN elements, at three different temperatures: -40C, 25C and **89C***

Impedance profile from the IC's perspective

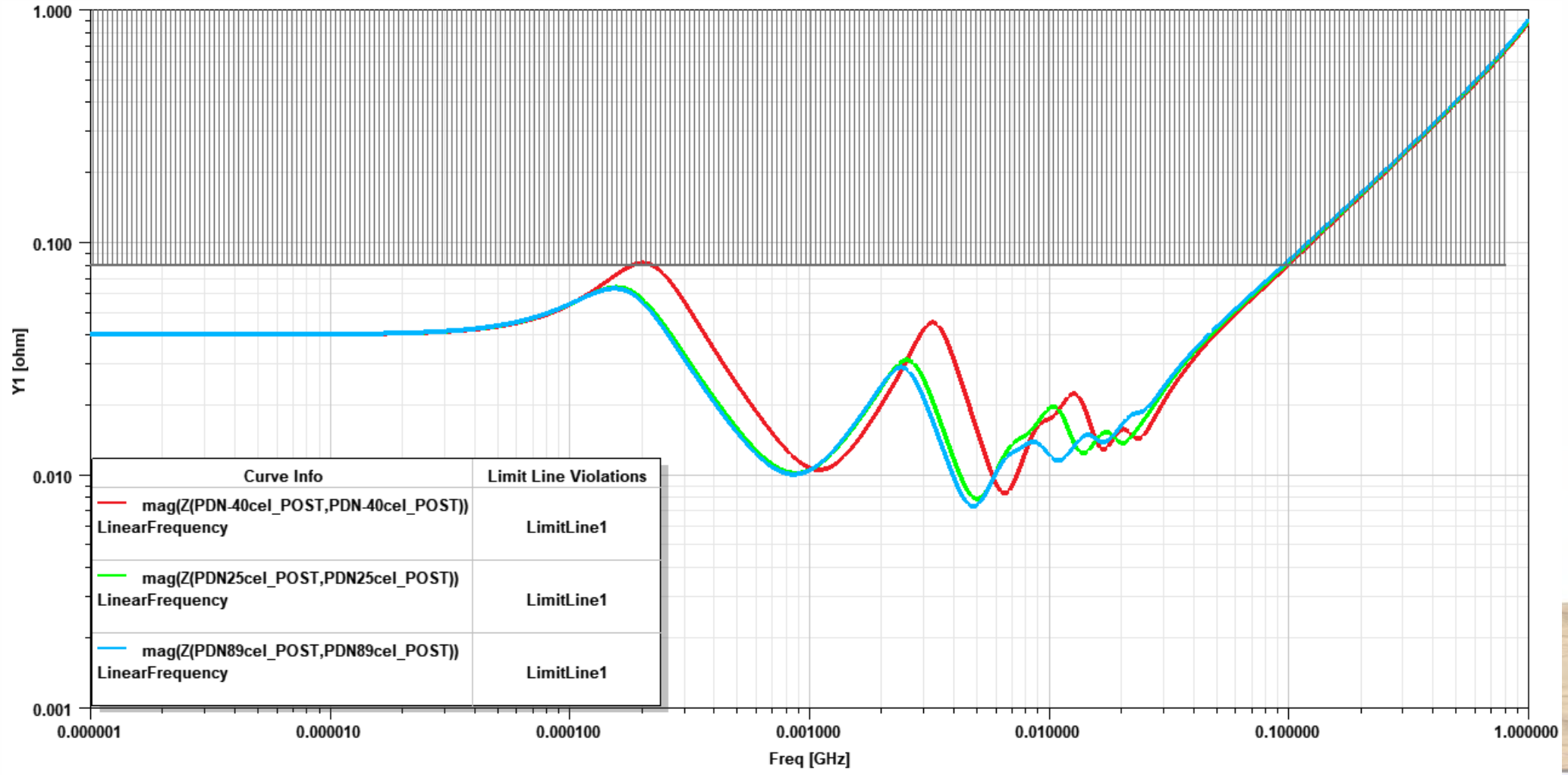
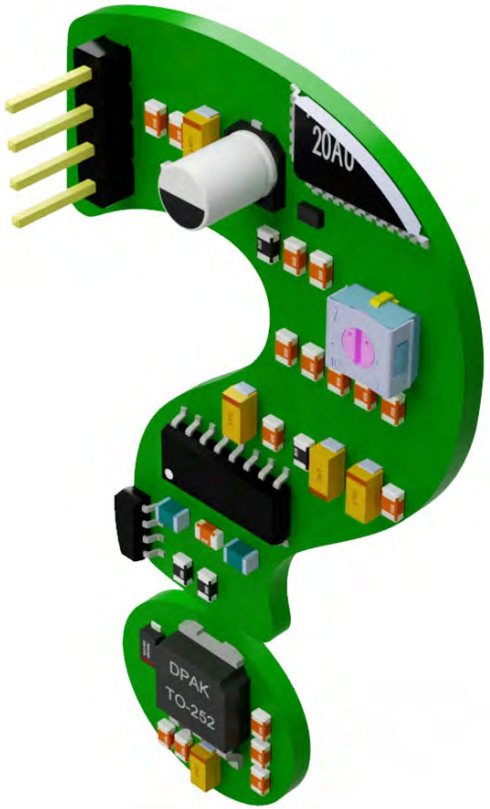


*Figure 24 – Impedance profile from the IC's perspective, parasitic elements extracted at three different temperatures: -40C, 25C and **89C***

7 Conclusions

- Thermal, Signal and Power integrity issues were addressed
- Simple analytical approximations provided a viable pre-layout analysis model

- Not all interface timing issues were addressed
- Routing could be improved for Sub-LVDS lines
- No PI analysis was performed for the 1V8 rail
- PDN for 1V1 and 1V8 rails under the BGA could be improved

Thank you for your attention!