DESIGN OF ELECTRONIC MODULES & ASSEMBLIES
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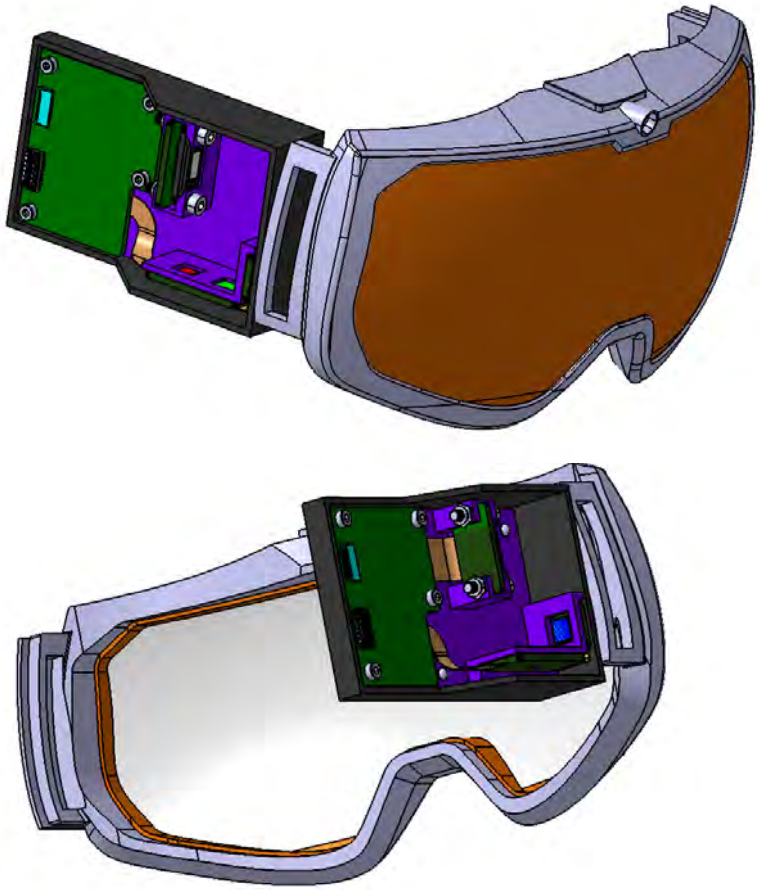
TIE 2020 – Online Edition



General description of the project:

This year's subject will bring into your attention, one of the most promising technologies in enhancing the human experience: ***Augmented reality***. To quote from Wiki: "***Augmented reality*** (AR) is an interactive experience of a real-world environment where the objects that reside in the real world are enhanced by computer-generated perceptual information, sometimes across multiple sensory modalities, including visual, auditory, haptic, somatosensory and olfactory."

The electrical schematic of the proposed concept is indicated in **Annex_1**.

System description:

- **DLPA2020 –** power management integrated circuit (PMIC) provides required low voltages for DLPC2020 and high voltages for DMD2020)
- **DLPC2020 –** main processor
- **OSRAM RGB LEDs –**light sources for the DMD2020
- **DMD2020 –** microelectromechanical(MEMS) optical projector mounted on a fine AXT540124 connector
- **SPI FLASH Memory**

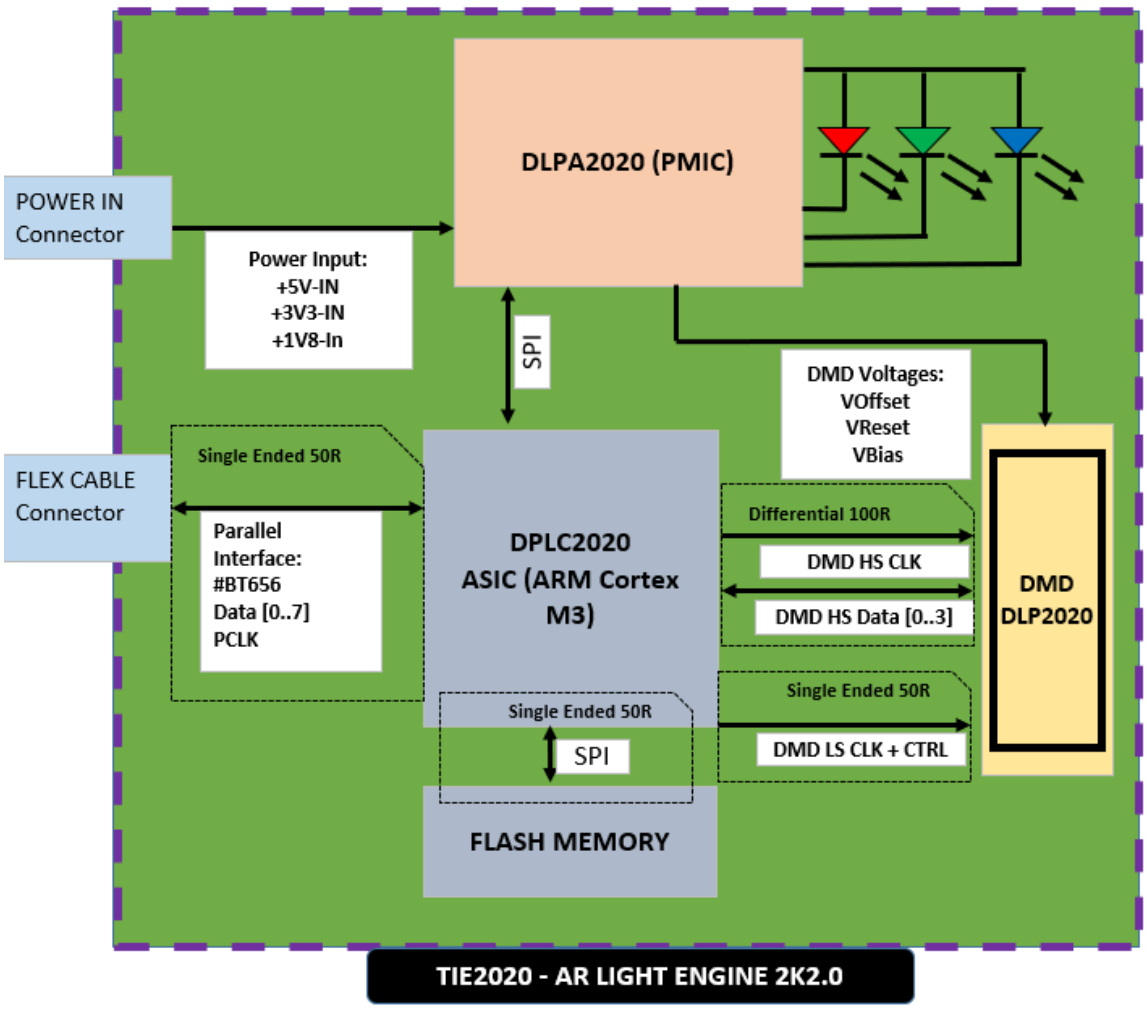


Figure 1. Block Diagram of the LIGHT ENGINE

Design flow and subject structure:

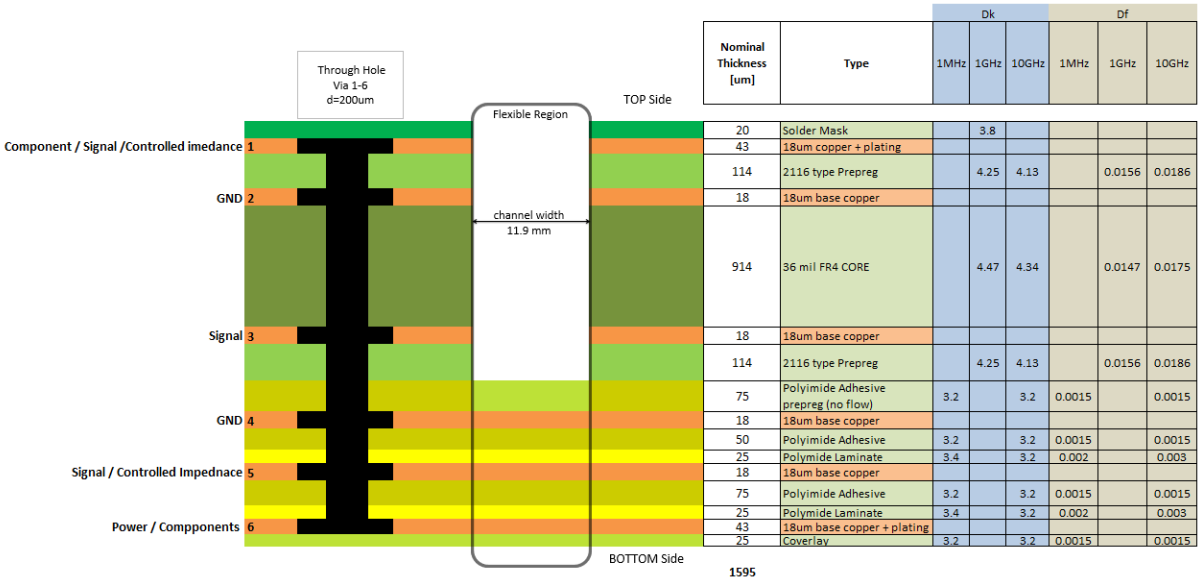
➔ ***The design order is mandatory***: libraries, schematic design, transfer procedure, layout design and postprocessing activities. ➔ The subject will be divided in ***three main parts***, each of them named intuitively ***TASK [1..3]***. The most important aspect is the fact that, each task will be ***unlocked after a precise timeframe***, this meaning that the student will not have a complete overview of the whole subject from the start.
All dimensions shall be considered in metric system.
TOTAL TIME 270minutes!

1. Schematic design and library creation - TASK [1]:

TSK-101	The schematic project will be created using any CAD system accepted in the contest (and respects all the minimum requirements published on the TIE official website).
TSK-102	Component descriptions, including standard footprints are indicated in the provided schematic and all the designers should have almost all of them ***complete before the actual contest.*** All used components ***must*** be inserted in a new library named ***TIE2020.***
TSK-103	The schematic ***must*** be drawn in a clear manner, strictly following ***Annex_1***: all reference designators, values and package type must have proper *value, size and orientation*, un-necessary crossings shall be avoided, no overlap of texts, graphical elements and electrical objects is allowed. The main purpose is to generate a correct netlist for PCB design, but it must also provide a clear representation of functionality. ***Special attention is required when importing the processor module with the adjacent components!***
TSK-104	The same ***page size*** shall be used as indicated in ***Annex_1***.
TSK-105	For testability reasons, ***test pads*** must be placed on ***power nets:*** *two test pads per net* including reference net (GND), having a copper pad diameter of 0.8mm and keeping the following distances: • **1mm test point to test point** • **0.5mm from any components.** For Video Parallel Interface each net, including BT656-PCLK, must contain a special test point (***bead probe***) with a rectangular geometry having a copper pad 0.15x0.3mm, keeping a distance of 0.5mm bead probe to bead probe and a distance of 1mm to all components, on bottom side. All standard test points must be placed on top side. **Due to the rigid flex design all test points must avoid the secondary rigid zones.**

TASK [2] will be unlocked after 60 minutes.

2. PCB technology definition and block placement requirements - TASK [2]:



	Nominal Thickness [um]	Type	Dk 1MHz	Dk 1GHz	Dk 10GHz	Df 1MHz	Df 1GHz	Df 10GHz
	20	Solder Mask		3.8				
1	43	18um copper + plating						
	114	2116 type Prepreg		4.25	4.13		0.0156	0.0186
2	18	18um base copper						
	914	36 mil FR4 CORE		4.47	4.34		0.0147	0.0175
3	18	18um base copper						
	114	2116 type Prepreg		4.25	4.13		0.0156	0.0186
	75	Polyimide Adhesive prepreg (no flow)	3.2		3.2	0.0015		0.0015
4	18	18um base copper						
	50	Polyimide Adhesive	3.2		3.2	0.0015		0.0015
	25	Polymide Laminate	3.4		3.2	0.002		0.003
5	18	18um base copper						
	75	Polyimide Adhesive	3.2		3.2	0.0015		0.0015
	25	Polymide Laminate	3.4		3.2	0.002		0.003
6	43	18um base copper + plating						
	25	Coverlay	3.2		3.2	0.0015		0.0015
	1595							

Figure 2. Proposed stack-up definition for the augmented reality system.

Due to the complexity of this monitoring unit, and the geometry of the housing, the unit must be designed using one ***rigid-flex PCB***. It contains ***4 rigid sides*** named intuitively **A, B, C and D**. Each one of these sides has its specific constraints and placement requirements.

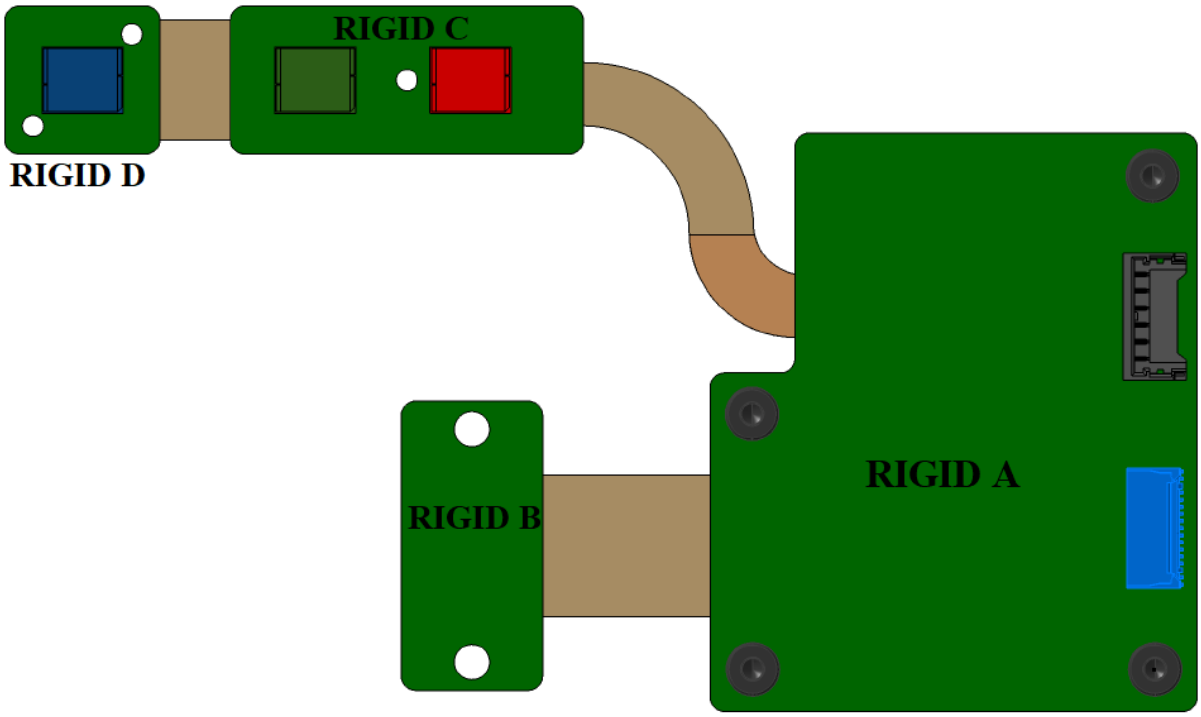
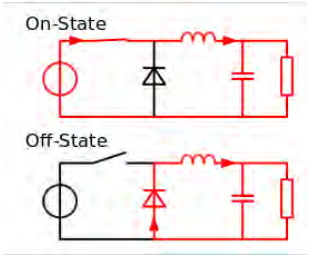


Figure 3. 2D view of the PCB and specific area naming.

<table>
<tr><td>TSK-201</td><td>The outline of the PCB must follow exactly the 2D data and the given dimensions. All the data will be imported in the CAD tool via the provided mechanical files and the restrictions will be defined via reference drawings.</td></tr>
<tr><td>TSK-202</td><td>The proposed stack-up definition was supplied by TIE+ contest and is fully described in Figure 2.
<u>Important remark</u>: if the CAD tool does not allow the definition of multiple isolation materials (for e.g. to differentiate polyimide from coverlay), the student must insert the total thickness of the isolation layers.</td></tr>
<tr><td>TSK-203</td><td>The project complexity dictates that the designer must use a rigid-flex PCB technology having the following requirements:
Minimum via dimensions: 200µm finished hole size and 400µm pad diameter
Minimum trace width: 85µm
Minimum trace spacing: 100µm
Minimum spacing component to component: 300µm
All PTH VIAs do not require solder mask opening definitions (except Thermal VIA)
All NPTH must have a minimum solder mask opening of 250µm defined
Board outline processing will be done at the PCB supplier using milling.</td></tr>
<tr><td>TSK-204</td><td>From signal integrity point of view the designer must take special care for the following lines:
Single ended 50R data lines and for Video Parallel Bus [BT656-D0..D7 + BT656-PCLK].
Single ended 50R data lines and for SPI interface between DLPC2020 and W25Q32JVTCI
Single ended 50R data lines and for low speed DMD command lines (DLP-LS-RD, DLP-LS-RST, DLP-LS-WD, DLP-LS-CLK)
Differential LVDS 100R DLP lines from DLPC2020 to DMD2020 (AXT540124).
Routing shall be done according to TIE+ contest results.
The relevant requirements provided will be as following:<table><tr><th></th><th>Routing Layers</th><th>Reference Layers</th><th>Trace width [µm]</th><th>Trace Spacing [µm]</th><th>Spacing to GND [µm]</th><th>Spacing to other nets [µm]</th></tr><tr><td rowspan="2">50Ω Single Ended Signals</td><td>1</td><td>2</td><td>180</td><td>N/A</td><td>250</td><td>300</td></tr><tr><td>5</td><td>4 / 6</td><td>80</td><td>N/A</td><td>250</td><td>300</td></tr><tr><td rowspan="2">100Ω Differential Signals</td><td>1</td><td>2</td><td>130</td><td>160</td><td>250</td><td>300</td></tr><tr><td>5</td><td>4 / 6</td><td>80</td><td>130</td><td>250</td><td>300</td></tr></table></td></tr>
<tr><td>TSK-205</td><td>Due to the sensitive nature of the optical engine the designer must consider the electrical current requirements for the LED power signals, LED_ANODE, LED-R-K, LED-G-K, LED-B-K, 2.4A max current.
For proper dimensioning of power lines use the attached calculation tool from ANNEX_3_Saturn.
If one does not want to use or cannot use the provided tool, the calculation is based on IPC-2152. Since the system is relatively dense, we strongly suggest using the “copper plane under the trace” option when doing the calculation. Provide a screen capture for the calculated value from the indicated tool.</td></tr>
<tr><td>TSK-206</td><td>The following components must have a fixed position (relative to the PCB origin defined in the mechanical drawing):
Connector X1 (x=0mm y=6mm)
Connector X2 (x=0mm y=25mm)
DMD2020 X3 (x=-48mm y=8mm)
LD1(x=-48.5mm y=41.8mm)
LD2(x=-59.5mm y=41.8mm)
LD3(x=-76mm y=41.8mm)
The Processor and PMIC (IC1 and IC2) shall be placed in such a way that the maximum specified length for data lines - single ended and differential pairs - shall not be exceeded. The power input for IC2 (PMIC) and the LED power lines must be as short as possible.
Please pay close attention the provided mechanical documentation to determine the correct placement layer.</td></tr>
</table>

TASK [3] will be unlocked after 60 minutes.

3. PCB routing and completion TASK [3]

TSK-300	Placement and routing must be done according to mechanical data and PCB stack-up!
TSK-301	When defining an EMC compliant product, the designer shall integrate the power supply (DLPA2020) in a similar manner as indicated in the reference design. It is mandatory to keep at minimum the ***Switching Loops*** and the ***Switching Nodes (SWx) and*** as short as possible (bellow 4mm distance between IC2 pin and coil pin) for the 3 DC-DC convertors integrated by the PMIC. Trace width for Coils connections must be 2 x PAD width of DLPA2020. Decupling capacitors must be places close to the corresponding IC pins as indicated in the schematic at less than 2mm.  ***Figure 4. Buck DC-DC Convertor (Wikipedia)***
TSK-302	**<u>Signal integrity requirements</u>** All relevant information regarding the specific trace routings will be provided by TIE+ contest results. 1. For single ended signals (50Ω) SPI FLASH + Parallel + LS DMD: • Maximum trace length: 25mm (VIDEO PARALEL) • Maximum trace length: 50mm (LS DMD) • Maximum trace length: 20mm (Flash) • Maximum VIA count per trace: 2 VIA • Maximum SKEW: ±2.5mm 2. For SLVDS differential signals (100Ω): • Maximum pair length 50mm • Maximum SKEW in pair: ±1mm • Maximum SKEW pair to pair: ±3mm • Maximum VIA count per trace: 3 VIA 3. For the following LS DMD signals a series resistor shall be added at less than 5mm to the driver, having a 43Ω value: • DLP-LS-RD (DLP2020, X3 is the driver) • DLP-LS-WD (DLPC2020, IC1is the driver) • DLP-LS-CLK (DLPC2020, IC1 is the driver) If possible, provide a layout report for the high-speed data lines detailing the implemented results.

TSK-303

Power integrity requirements:

All relevant information regarding the specific trace routings are provided from TIE+ contest results.
Due to Simulation analysis results update the number and types of decupling capacitors for IC1 (DLPC2020) as indicated in the following table:

Power Net	Capacitors Per Pin Cluster @IC1 DLPC2020	Capacitors Per Pin Cluster @X3 DLP2020
+1V1-OUT	6x100nF (0402), 4x220nF (0402), 1x1µF (0402), 2x4.7µF (0603)	N.A.
+1V8-OUT	4x100nF (0402), 1x 1µF (0402)	6x100nF (0402)
+3V3-IN	5x100nF (0402)	N.A.

Each decupling capacitive structure must be placed as close as possible to it is corresponding power rail. To avoid SI/PI and EMC issues the PLL power supply decupling capacitors must be placed as indicated in the schematic.

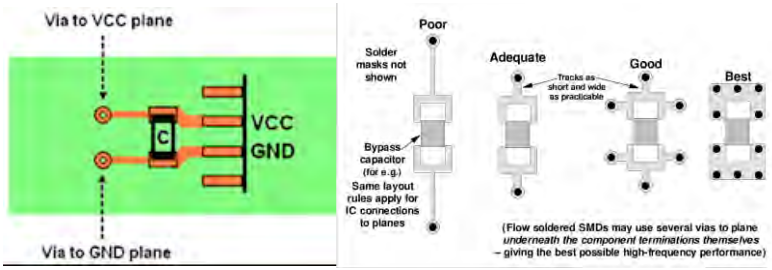


Figure 5. Pictures for reference routing strategy only!

TSK-304

The DLPA2020 QFN has an exposed thermal pad as indicated in the footprint drawing. To properly dissipate the heat from the case, calculate the minimum relevant number of thermal VIAs.
Temperature drop from junction to PCB bottom (under component) should be less or equal to ***22 °C***.

Use Thermal Via with ***300µm*** hole size and ***600µm*** copper pad, without solder mask and implement it in the PCB design. IC2 (DLPA2020) dissipates a power of ***1.6W***. The thermal resistance for one VIA 300µm is ***167.5°C/W***.

Provide a document with the task name for the calculated thermal resistance of the heat path. Any format is accepted.

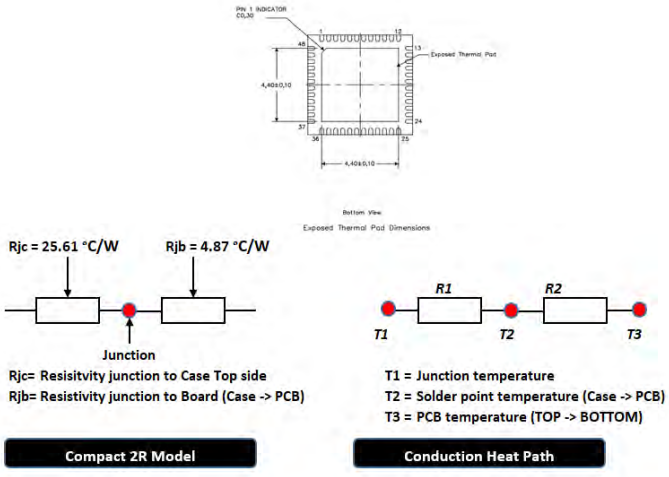


Figure 6. 2R model for IC2(DLPA-2020)

TSK-305	Calculate the heat path for one LED and chose the appropriate heatsink to keep the junction temperature in a safe operating area (20°C below maximum accepted) considering natural convection. To efficiently extract the heat dissipated by the 3 LEDs create a low thermal impedance trough the PCB by implementing Copper inlays under each LED, followed by a local heatsink. *According to Wikipedia copper inlay represents an additional PCB manufacturing stage, were a small copper "coin" is inserted in the PCB under each component for which classic thermal VIA is insufficient, as specified by the design data.*

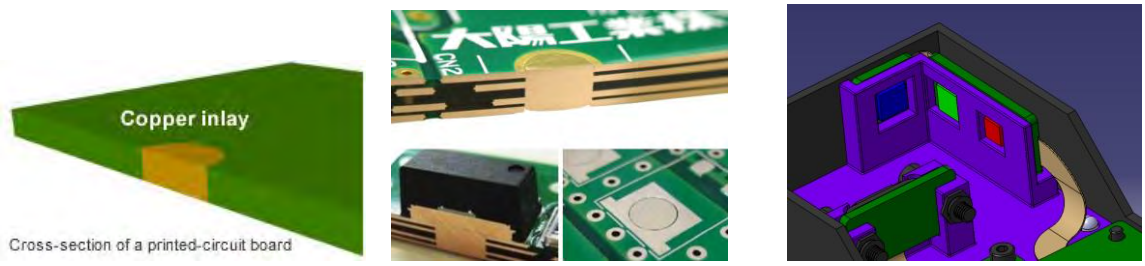
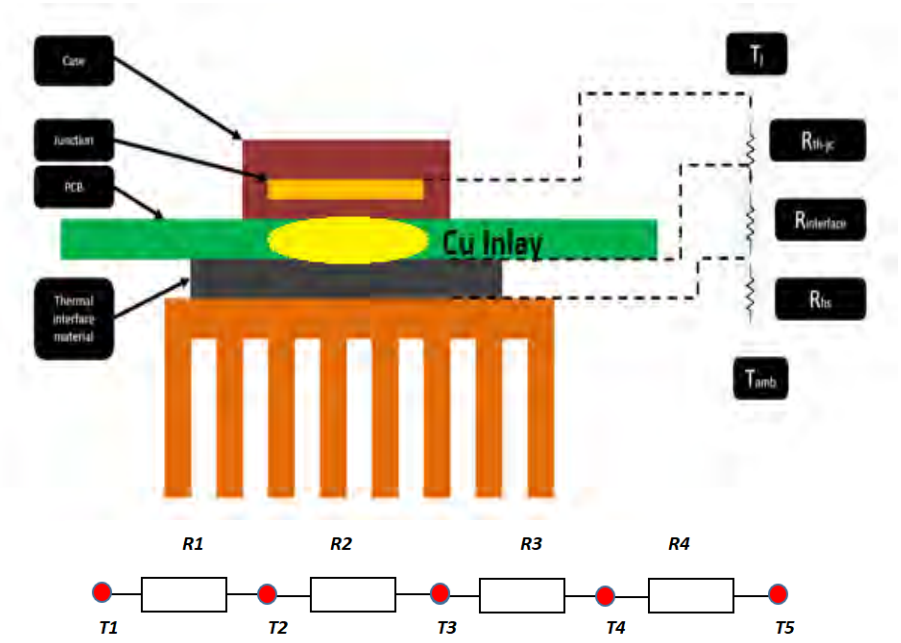


Figure 7. Detailed view of Copper Inlay Process (Wikipedia)

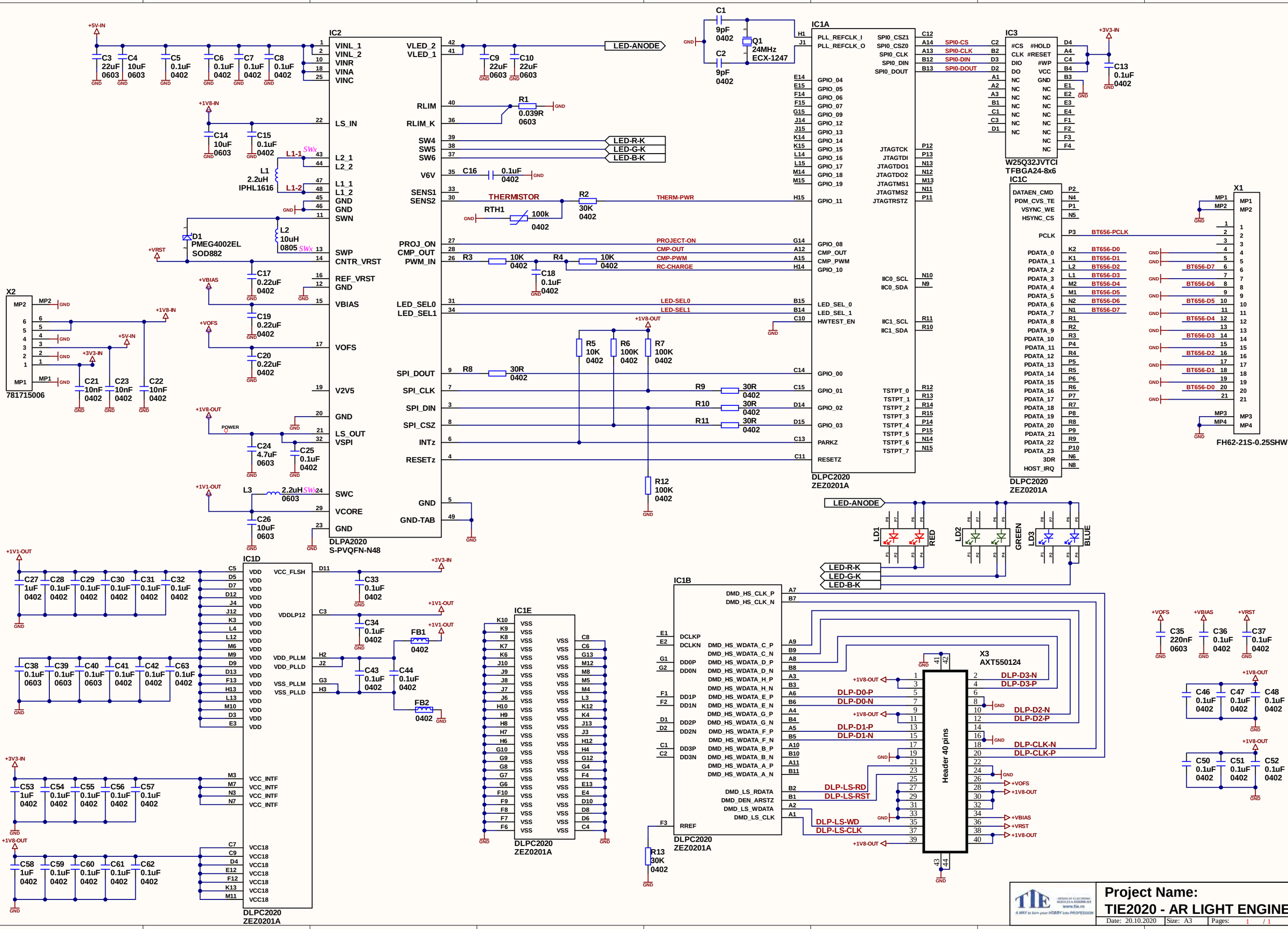


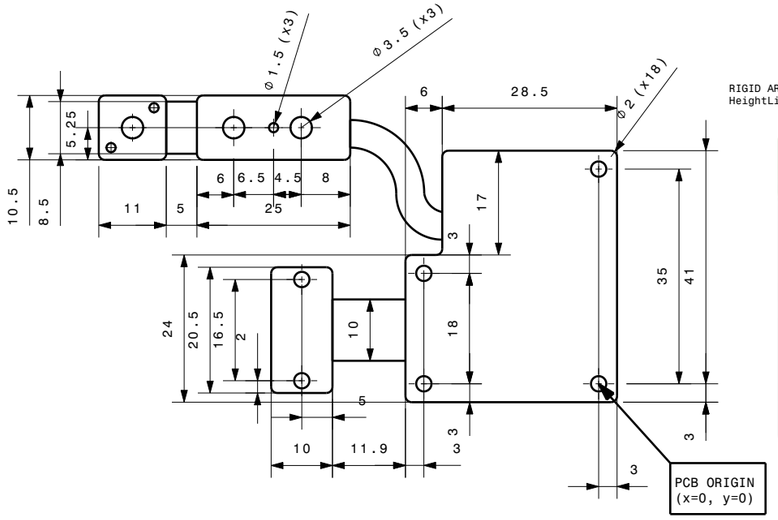
T1 = Junction temperature
T2 = Solder point temperature
T3 = PCB temperature (bottom side of PCB)
T4 = Heatsink temperature (contact with TIM)
T5 = Ambient temperature

Figure 8. Conduction Heat Path for one LED

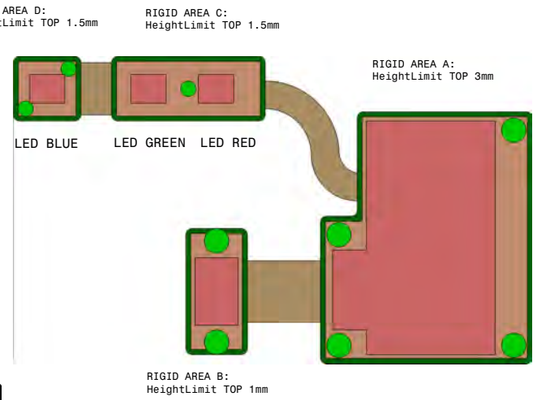
	The Copper insert and exposed copper from bottom side equal to the TIM area of the PCB under each LED will be in contact with a heat sink trough a thermal interface material (TIM, see ANNEX-4Tflex-SF800.pdf). The TIM has its own thermal resistance and shall be calculated using the formula: $Rth = \frac{L}{K \cdot A_s}$ Rth = TIM thermal resistivity K = Thermal Conductivity L = Length of the TIM [m] As = cross section area where heat is applied [m^2] LED thermal resistance junction/solder point: 1.3 °C/W Copper thermal conductivity: 385 W/m°C Copper Inlay coin diameter: 3.5mm TIM dimensions: 7x7x0.8mm Ambient temperature: 55°C Maximum accepted junction temperature: 150°C LED Power dissipation: 3.3W / LED For Heatsink options see ANNEX_5! Provide a document with the task name for the calculated thermal resistance of the heat path. Any format is accepted.
TSK-306	Define one „documentation" layer that will be generated in Gerber format, which will contain all the PCB outline dimensions indicated in the drawing and a clear indication of the rigid / flex and copper inlay areas. This is necessary for the manufacturer to clearly understand our needs.
TSK-307	The necessary fabrication files (in extended Gerber format) must be provided.
TSK-308	Distinct drill file for holes must be provided.
TSK-309	Pick-and-place file for all SMT components must be generated and must contain component reference, position x, position y and rotation.
TSK-310	A list of test point co-ordinates must be created in .csv or .txt format.
TSK-311	A list of components (BOM) must be generated in .csv or .txt format, and must contain the following details: Component Reference, Part Name/Value and Package.

TASK [3] - Total time - 150 minutes.

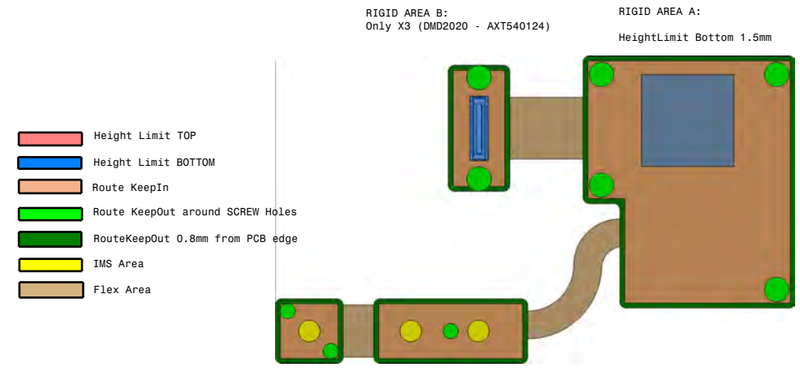

IC2
DLPA2020
S-PVQFN-N48
IC1A
DLPC2020
ZEZ0201A
IC1B
DLPC2020
ZEZ0201A
IC1C
DLPC2020
ZEZ0201A
IC1D
DLPC2020
ZEZ0201A
IC1E
DLPC2020
ZEZ0201A
IC3
W25Q32JVTCI
TFBGA24-8x6
X1
FH62-21S-0.25SHW
X2
781715006
X3
AXT550124
Header 40 pins
LED-ANODE
LED-R-K
LED-G-K
LED-B-K
THERMISTOR
Q1
24MHz
ECX-1247
Project Name:
TIE2020 - AR LIGHT ENGINE
Date: 20.10.2020
Size: A3
Pages: 1 / 1



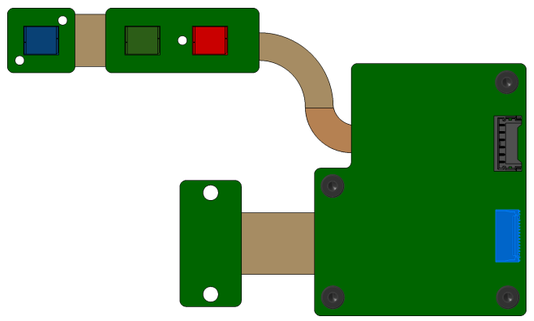
TOP View
PCB Outline
Scale: 1:1



Restrictions for TOP Side
Scale: 1:1

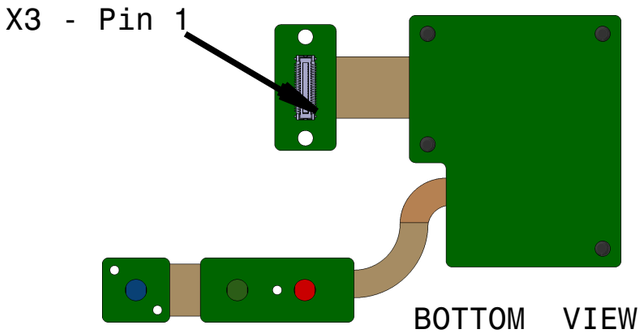


Restrictions for Bottom Side
Scale: 1:1

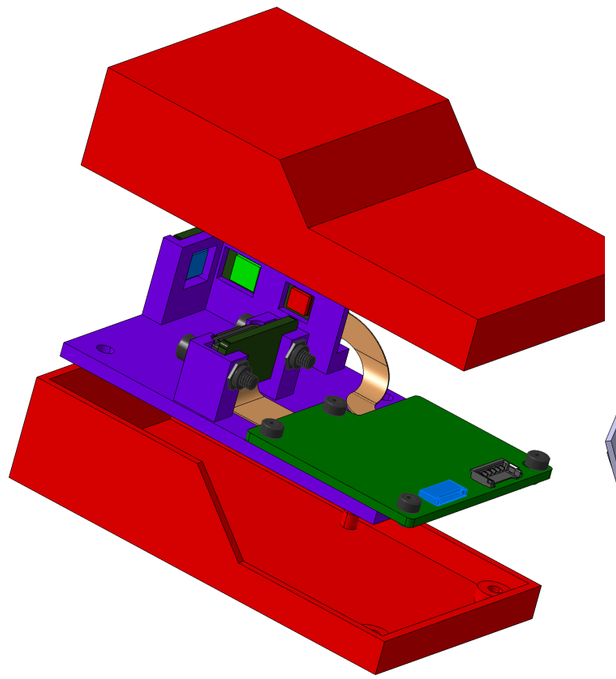


- Connector X1 (x=0mm y=6mm)
- Connector X2 (x=0mm y=25mm)
- DMD2020 X3 (x=-48mm y=8mm)
- LD1(x=-48.5mm y=41.8mm)
- LD2(x=-59.5mm y=41.8mm)
- LD3(x=-76mm y=41.8mm)

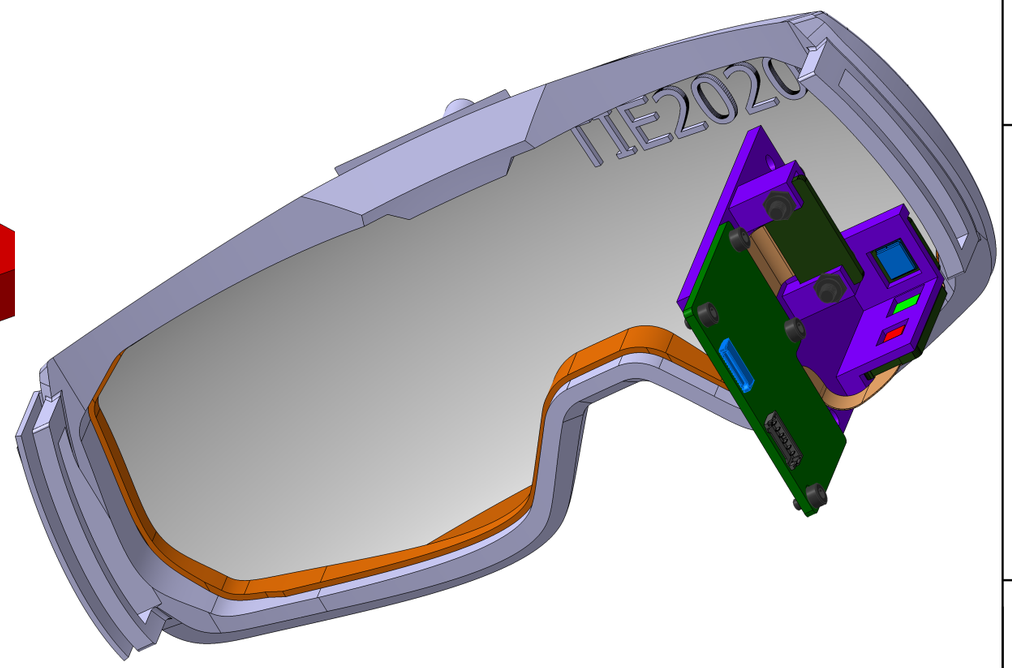
TOP VIEW COMPONENTS
Scale: 1:1



BOTTOM VIEW COMPONENTS
Scale: 1:1



Isometric view
Scale: 1:1



Isometric view
Scale: 1:1

SIZE	DRAWING NUMBER	REV
A3	TIE2020	X
SCALE 1:1		SHEET 1/2